Three-Level Current-Source PWM Inverter with No Isolated Switching Devices for Photovoltaic Conditioner

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Keywords: current-source inverter, common-source, photovoltaic conditioner

This paper presents a new configuration of a three-level current-source PWM inverter (CSI) with a fully common-source topology in terms of all FET switching devices. Using this common-source CSI, the number of gate drive power supplies can dramatically be reduced by using only a single power supply instead of a conventional bootstrap circuit or isolated power supplies. As a result, it can eliminate expensive transformers of isolated power supplies and capacitors of bootstrap circuit in the drive circuits of the switching devices. In addition, the circuit can be operated at a higher switching frequency and a higher voltage because of its common-source topology.

Fig. 1 shows the circuit diagram of proposed three-level current source inverter circuit. In this circuit, all of the power switches are connected at common-source or common emitter. The inverter circuit is connected with a photovoltaic simulator modeled by a simple DC voltage source (Vdc) connected in series with its internal resistance (Rin) based on the condition that the optimum current of photovoltaic is proportional with the short-circuit current of its output terminal. Blocking diodes are placed between the input inductors and the negative terminal of the DC voltage source in order to prevent the current from flowing back during positive and negative cycles of inverter current generation.

Basically, the circuit consists of two buck-chopper circuits with common control switch Q1 and a PWM inverter circuit. The chopper circuit works generating current sources, where during positive and negative cycle of the inverter output current, a part of the input inductor current ($I_{Lin)}$ will flow back through the blocking diode (I_D) while the switch Q1 is turned-on and the remaining current (I_L) will flow into the inverter during the switch Q1 is turned-off. The switching gate signal of the switch Q1 (dc-to-dc switch) is generated by comparing the error signal of the average value of detected steady state current flowing through both of the input inductors I1 and I2, and a triangular carrier wave after passing through a proportional integral (PI) regulator. This signal is used to control the duty cycle of the chopper to get balanced input inductor currents I1 and I2.

Sinusoidal pulse width modulation (sinusoidal-PWM) is used to generate the gating signal for three-level output current pattern with 50 Hz line-frequency. The sinusoidal PWM is generated by using a sinusoidal reference wave modulated with two triangular carrier waves with the same frequency but with opposite offset values. This strategy is able to perform the sinusoidal PWM of the inverter. These signal patterns are used to control the inverter switches Q2, Q3, Q4, and Q5. Fig 2 shows the overall controller diagram of the chopper and inverter circuit.

Fig. 3(a) and 3(b) show the experimental result of three-level output current waveform and its waveform after filtering, respectively. The total harmonic distortion of this three-level output current is 5.48% and 0.67% for the filtered waveform.

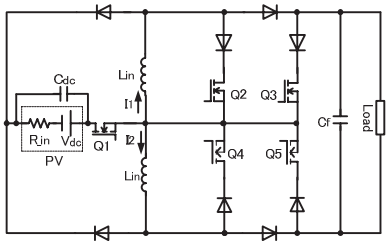


Fig. 1. Proposed common-source three-level CSI circuit

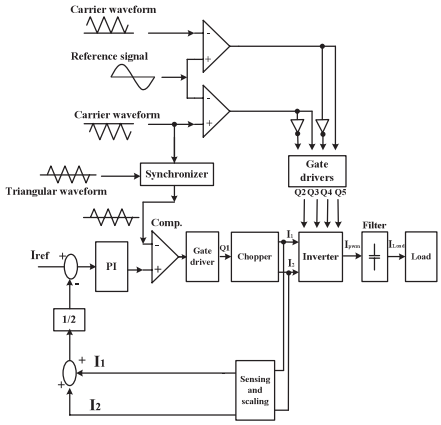
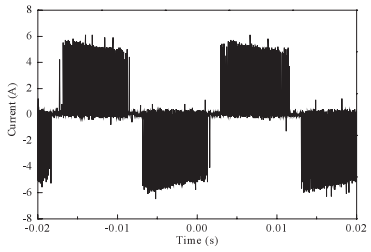
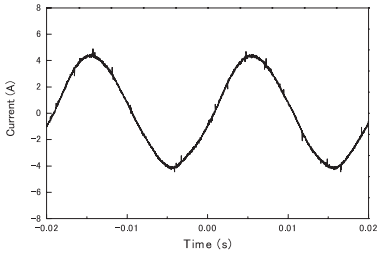


Fig. 2. Block diagram of current controller



(a) Three-level output current waveform.



(b) Three-level output current waveform after filtering.

Fig. 3. Experimental waveforms of proposed inverter circuit

Paper

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This paper presents a new configuration of a three-level current-source PWM inverter (CSI) with a full common-source or common-emitter topology in terms of all transistor switching devices. Using this new configuration, the number of gate or base drive power supplies can dramatically be reduced to only a single instead of use of several isolated power supplies or conventional bootstrap circuits. As a result, bulky, heavy and expensive transformers and capacitors in the drive circuits are eliminated. In addition, the proposed configuration is capable to be operated at a higher switching frequency and a higher voltage without violent potential changes because of its common-source or common-emitter topology. Design and operation principle of the new circuit are investigated and analyzed using computer simulations. Finally, effectiveness of the circuit is experimentally verified by using a laboratory prototype set up. The simulation and the experimental results show that the circuit works properly to generate a three-level output current waveform, which proves feasibility of the proposed approach.

Keywords: current-source inverter, common-source, photovoltaic conditioner

1. Introduction

In recent years, distributed renewable power generation systems are more and more popular from the viewpoint of environment and energy conservation issues. Photovoltaic (PV) solar systems are very promising and interesting alternatives to supplement the generation of electricity among green energy sources because they can be utilized either at remote regions as stand alone apparatus or at urban applications with a grid interactive connection [1][2].

On the other hand, owing to continuing development of power devices working at a high switching-frequency for medium and high power applications such as MOSFETs, IGBTs and IGCTs, overall performances of power converters have significantly been improved. Particularly, multilevel inverter topologies are taking great attention because they can effectively reduce harmonic distortion of the output waveforms. It goes without saying that the multilevel inverters are very attractive even in PV power conditioning applications, compared with traditional two-level PWM inverters [3][4].

A voltage-source inverter (VSI) such as a three-level neutral-point clamped (NPC) inverter is conventionally used as a PV power conditioner either for the grid interactive or the standalone operation. This system, however, has limitation when used in high-voltage and high-switching-frequency applications because of an EMI noise problem caused by high-dV/dt of the switching devices used. On the other hand, a current-source inverter (CSI) has some advantages compared with the VSI, e.g., no need of an interconnecting inductor when used for the grid interactive application, direct controllability of the output current without current control loops, inherent short-circuit current durability and longer lifetime of its reactors if compared with electrolytic capacitors used in the VSI.

In order to make technical breakthrough to overcome the above problems, innovative PV power conditioning circuits should newly be created for both of the standalone and the grid interactive systems. General and basic circuits of the new topology based multilevel CSI have been discussed in Ref. (5). Reference (6) reports new multilevel CSIs driven by a single gate power supply merely at the inverter part. However, the power switching devices of the chopper circuits, which consist of DC current power sources, still need some isolated drive circuits.

In this paper, a novel three-level CSI circuit, which achieves complete common-source or common-emitter topology throughout the DC current power source to the AC output stage is presented. Using this topology, the number of gate drive power supplies can dramatically be reduced to only a single to drive all power switching devices without isolated power supplies or conventional bootstrap circuits. In addition, the circuit can overcome the above mentioned dV/dt issue of the system; hence the proposed circuit can be operated at a higher switching frequency for better quality of the output current waveforms. The principle of the proposed CSI operation is investigated and examined through computer simulations prior to experimental tests. Furthermore, an prototype circuit is set up to verify experimentally performance of the proposed topology, using some power MOSFETs.

2. Circuit Topology and Operation Principle

2.1 Outline of Circuit Topology One of the main goals of the PV power conditioner is to process the PV power into a sinusoidal current injected into the utility grid in the application of the grid interaction. Such a low distorted current

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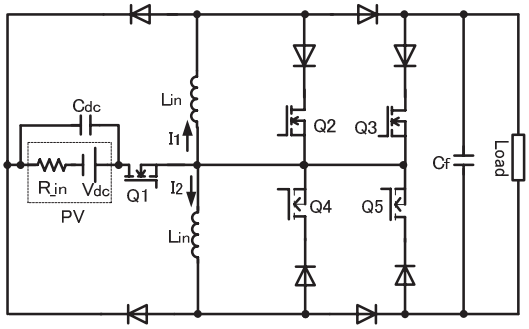


Fig. 1. Proposed three-level CSI with common-source topology

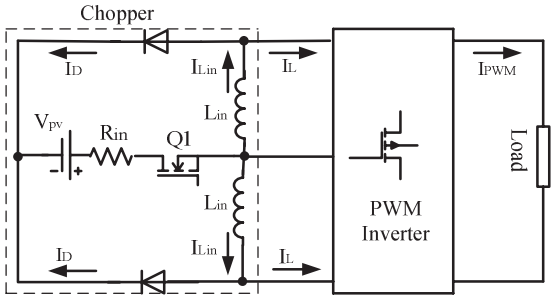


Fig. 2. DC current-sources composed by chopper with common-source switching device Q1

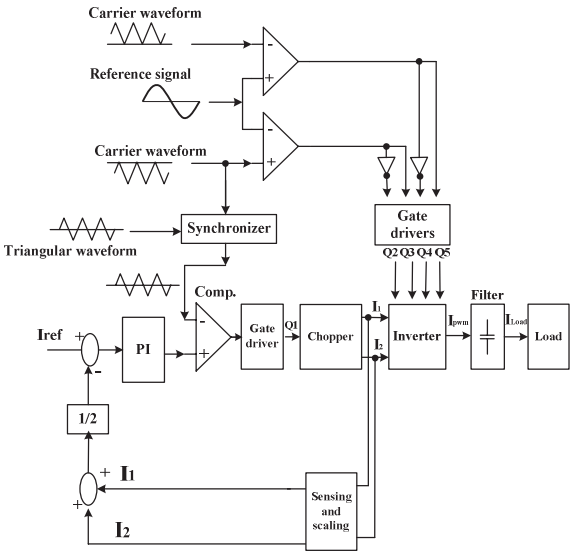


Fig. 3. Block diagram of current controller

can be obtained, using the proposed new topology. Figure 1 shows the proposed three-level CSI with full common-source topology. The current sources, at the input of the DC-to-DC converter, are composed by some PV arrays connected to the input inductors L_{in}. Since an optimum current of the PV is determined by its short-circuit current, photovoltaic can be modeled by a simple DC voltage source V_{dc} connected with a series internal resistance R_{in} [7][8]. A power decoupling capacitor C_{dc} is also connected across the output terminals of the PV arrays to reduce the voltage ripple caused by R_{in}. Blocking diodes are inserted between L_{in} and the negative terminal of C_{dc} in order to prevent the current from flowing back during positive and negative cycles of inverter current generation.

A unique point of the proposed three-level CSI circuit is that all of the switching devices are operated on an exactly identical potential level, where all the sources commonly connected [9]. Using this new inverter topology, the following advantages over the conventional one can be obtained:

(1) Using this circuit topology, the number of the gate drive power supply can be reduced to only a single without using isolated power supplies or a bootstrap technique. Hence, the circuit can effectively reduce circuit components in the drive circuits such as transformers, which are indispensable for electrical isolation, or can reduce capacitors required for bootstrap based circuits.

(2) All the switching devices are connected at the identical reference potential level; hence the proposed circuit can avoid the EMI noise problem caused by high dV/dt switching operation. Moreover, it is possible to operate the circuit at a considerably high switching frequency in order to obtain a low-distorted inverter output current waveform by pushing up the dominant harmonic components into a higher frequency range. In addition, a smaller output filter can be used to eliminate the output ripples because of the higher switching frequency.

2.2 Chopper Circuit For an analytical purpose of the buck chopper used in the proposed circuit as DC current power sources, it is reasonable to consider that this circuit comprises two buck choppers with commonly controlled switching device Q1 as shown in Fig. 2. The chopper behaves as a current source during a positive and a negative cycle of the inverter AC output stage, where a part of the input inductor current I_{Lin} flows back through the blocking diode I_D while Q1 is on, and the remaining current I_L flows to the inverter during off-state of Q1.

A current control is applied to regulate the currents delivered to the input inductors L_{in} and the amplitude of the output current I_{PWM} simultaneously. Making the input inductors current I_{Lin} and the output current I_{PWM} follow the reference current I_{ref} is the objective of the current controller. The switching gate signal of Q1 is generated by comparing the error signal between the average value of detected steady state current flowing through both of the input inductors I1 and I2, and a triangular carrier wave after passing through a proportional-integral (PI) regulator. This signal is used to control the duty cycle D of the chopper to obtain the commanded and balanced input inductor currents I1 and I2. In order to avoid uncontrolled situations of the output current by modulation signal during the on-state of Q1, the switching timing between Q1 and the switching states of the inverter must be synchronized as shown in Fig. 3. A well-known sinusoidal PWM technique is employed to generate the gating signals of the inverter switching devices Q2 to Q5.

The input inductor current I_{Lin}, the gating signal V_{gate} of the chopper switching device Q1 and the current flowing into the inverter I_L are shown in Fig. 4 with the assumption that the current rises and falls linearly. As a matter of fact, the current varies according to the time constant of the circuit, but generally this time constant is much longer than the switching period. Thus, a linear approximation is valid enough to simplify expressions of the circuit.

When Q1 is turned-on for a period of DT, the input inductor is energized by photovoltaic energy to its maximum energy W, which is expressed as

$$W = \frac{1}{2} L_{in} I_{Lin}^2 . \cdots\cdots (1)$$

The on-state circuit or an energy charging mode of the inductor is represented in Fig. 5(a). In case of pure resistive load R_L, the input inductor current I_{Lin} is expressed as

$$I_{Lin} = \frac{V_{pv}}{R_{in}} (1 - e^{-\frac{R_{in}}{L_{in}} t}), \cdots\cdots (2)$$

where V_{pv} and R_{in} are the terminal output voltage and the series internal resistance of the photovoltaic arrays, respectively.

The current increases almost linearly to its maximum value, depending on V_{pv} and R_{in}. In this calculation, an internal resistance of the input inductor is neglected because its value is much smaller than R_{in}.

The energy is stored in a magnetic field of the input inductor, and when Q1 is turned-off during (1 − D)T, the stored energy is released to the load via the inverter circuit as a PWM current. The energy-discharging mode of the input inductor in this circuit can be represented by Fig. 5(b). From this figure, the current flowing into the inverter I_L can be expressed as

$$I_L = i_{L0} e^{-\frac{R_L}{L_{in}} t}, \cdots\cdots (3)$$

where i_{Lo} is the initial current flowing through the input inductor. From this equation, it can be found that the current decreases, depending on the time constant determined by L_{in} and the load resistance R_L. Based on the charging and discharging modes of the input inductor as shown in Fig. 4 and Fig. 5, the input inductor size can be expressed as follows:

$$L_{in} = \frac{(1 - D) T V_{in} R_L}{R_{in} \Delta i}, \cdots\cdots (4)$$

where Δi is an acceptable current ripple. From the above equation, it is seen that the input inductor size can be reduced by increasing the switching frequency of the chopper. As the inductor size and/or switching frequency increase, the current ripple decreases. In addition, the two current amplitudes of the DC current power sources must equally be regulated by the current controller. Only a single switching device is, however, available to control the input inductor currents although the two currents are simultaneously detected by Hall-effect CTs. Therefore, it is necessary to determine the input inductance at a relatively high value to keep a current balance, e.g., hundreds mH.

2.3 Inverter Circuit and Modulation Method The inverter part consists of four controlled switching devices and six diodes as shown in Fig. 6, where I1 and I2 represent average input inductor currents in the steady state. The diodes connected in series with the switching devices are used to protect them from transient voltages due to the load current switching. Sinusoidal PWM method is employed to generate the three-level output current pattern of which frequency is 50 or 60 Hz as shown in Fig. 7.

The gating signals of the inverter are generated by using a sinusoidal reference wave modulated with two triangular carrier waves with the same frequency but with opposite offset values. These signal patterns are used to control the switching devices Q2 to Q5. The frequency of the reference signal determines the output current frequency of the inverter and

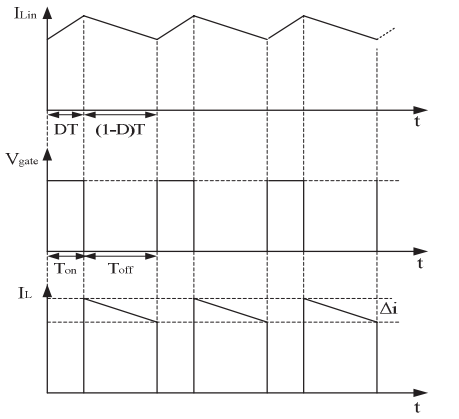
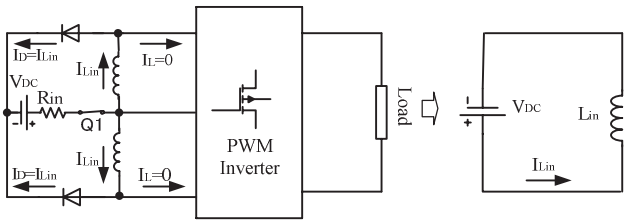
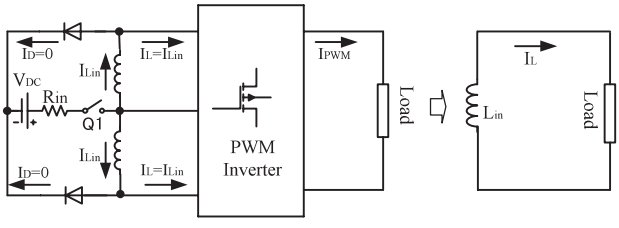


Fig. 4. Operation waveforms of chopper



(a) Energy charging mode of input inductor.



(b) Energy discharging mode of input inductor.

Fig. 5. Operation modes of chopper

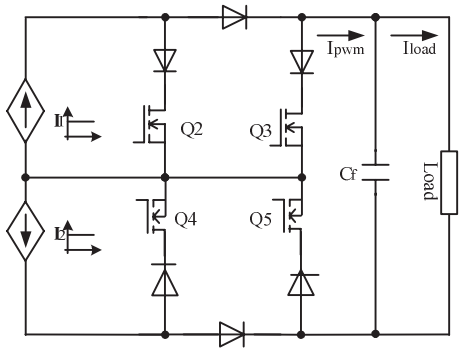


Fig. 6. Circuit model of proposed three-level CSI

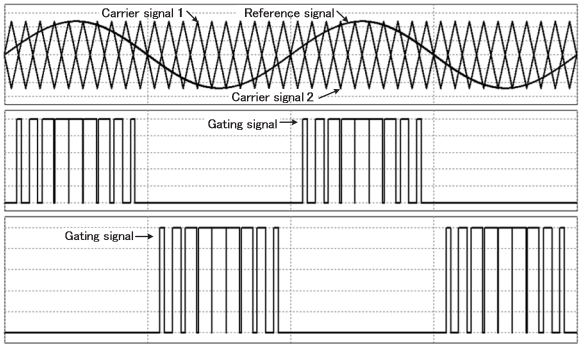
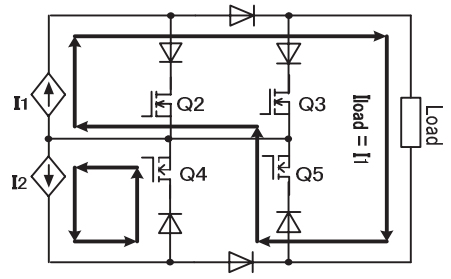
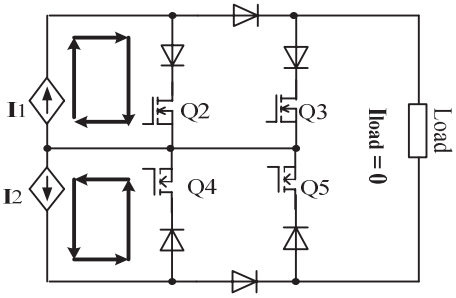


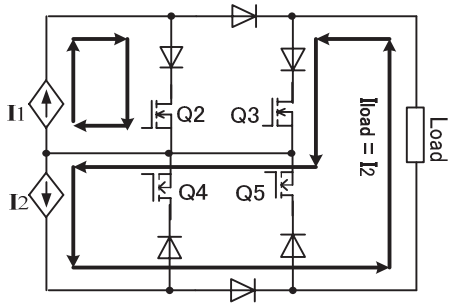
Fig. 7. Sinusoidal PWM for three-level current generation



(a) Switching state for positive-level load current generation.



(b) Switching state for zero-level load current generation.



(c) Switching state for negative-level load current generation.

Fig. 8. Operation modes of proposed three-level CSI

Table 1. Switching states of proposed three-level CSI

Output current	Switching states			
	Q2	Q3	Q4	Q5
Positive-level	0	0	1	1
Zero-level	1	0	1	0
Negative-level	1	1	0	0

its magnitude can be controlled by the amplitude of the fundamental current command.

The current paths and switching combinations required to generate this three-level current waveform are indicated in Figs. 8(a) to 8(c). The required three-level output current (positive, zero and negative levels) are generated as follows:

(1) Positive-level load current generation: Q5 is turned on, connecting the input inductor current I1 to the load. Q4 is also turned on, making the current path for input inductor current I2. However, Q2 and Q3 are turned off.

(2) Zero-level load current generation: Q2 and Q4 are turned on, making the current circulation path for current I1 and I2, respectively. Q3 and Q5 are turned off.

(3) Negative-level load current generation: Q3 is turned on, connecting the current I2 to the load. Q2 is also turned on, making the current path for input inductor current I1. However, Q4 and Q5 are turned off.

The switching states of the inverter are summarized in Table 1. The switching frequency of the inverter is chosen to achieve low noise as well as small harmonic components of the AC output current and a smaller size of an output current filter to obtain a sinusoidal voltage waveform across the load.

Table 2. Circuit parameters and test conditions

Components	Parameters
Input voltage	120 V
Series internal resistance of PV	10 Ω
Input inductor	100 mH
Decoupling capacitor of PV	220 μF
Chopper switching frequency	10 kHz
Inverter switching frequency	30 kHz
Output filter capacitor C_f	220 μF
Load R_L and L_L	R_L = 5.5 Ω L_L = 3.4 mH
Modulation Index	0.9

3. Computer Simulation Results

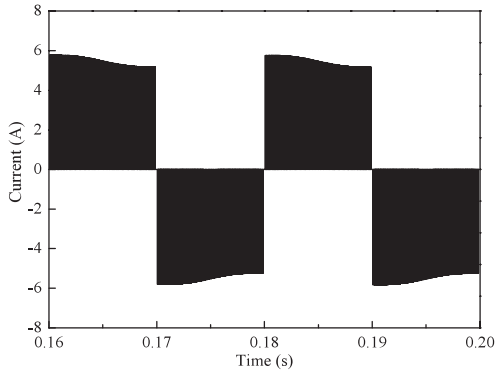
This section describes some computer simulation results of the proposed three-level CSI with common-source topology. In order to analyze and to test the proposed topology, the circuit was simulated by using PSIM software. The simulation parameters are listed in Table 2. In this simulation, the PV, which acts as a power source of the circuit, is represented by a DC voltage source connected with its series internal resistance, and the inverter is connected to an output filter capacitor C_f and an inductive load L_L and R_L. The input inductors are chosen to be 100 mH to obtain smooth and well-balanced enough input inductor current I1 and I2. It should be noted that the inverter also works for a smaller value of the input inductors.

The inverter generates a three-level output current as shown in Fig. 9(a), of which output frequency is 50 Hz. A decoupling capacitor used in this simulation is 220 μF. The harmonic spectra of the three-level output current calculated with FFT algorithm is shown in Fig. 9(b). From the FFT analysis result, it can be seen that most of the harmonic components are less than 1% except for the 3rd harmonic component, which is also as small as 3%. Fig. 9(c) shows the load current, which is almost a perfect sinusoidal waveform after filtered by the capacitor C_f. Fig. 9(d) presents the frequency spectra of the load current, and the harmonic components of the load current are effectively rejected by the output filter capacitor of 220 μF.

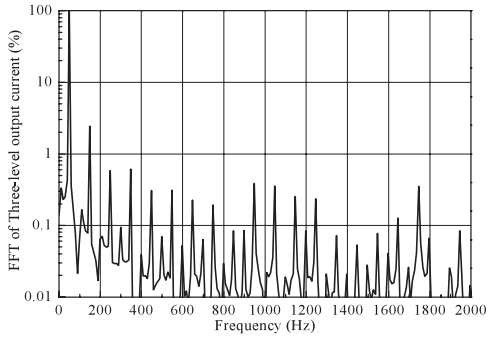
4. Experimental Results

In order to verify proper operations and to prove feasibility of the proposed configuration, a laboratory prototype was set up by using 300-V 30-A FK30SM-6 power MOSFETs and 1200-V 16-A HFA16PB120 fast recovery diodes. The experimental circuit specifications are identical with the simulation parameters listed in Table 2. Fig. 10 shows the experimental result, where the three-level output current waveform is indicated in Fig. 10(a). Its FFT analysis result is shown in Fig. 10(b). As can be seen in these results, most of the harmonic amplitudes are less than 3%, which is slightly higher that that of simulation result.

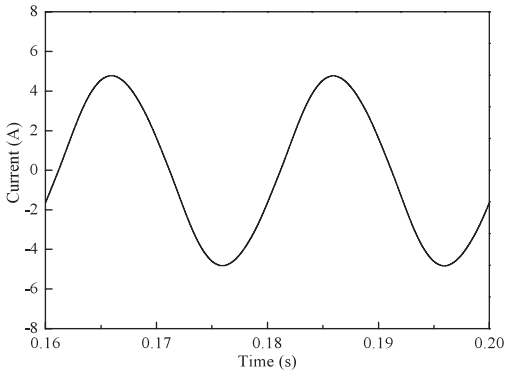
The total harmonic distortion (THD) of the three-level output current is 5.48%. Figs. 10(c) and 10(d) show the load current after filtering and its frequency spectra, respectively. The current waveform is almost perfect sinusoidal with very



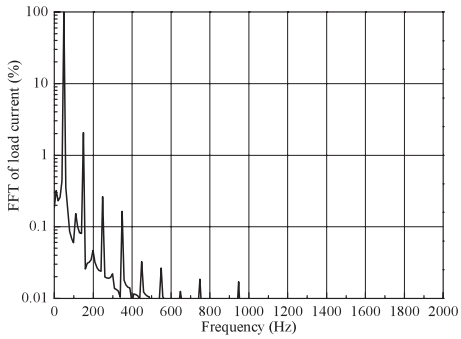
(a) Three level output current waveform.



(b) Frequency spectra of three-level output current

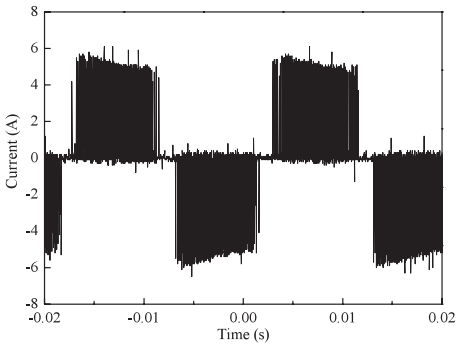


(c) Load current waveform.

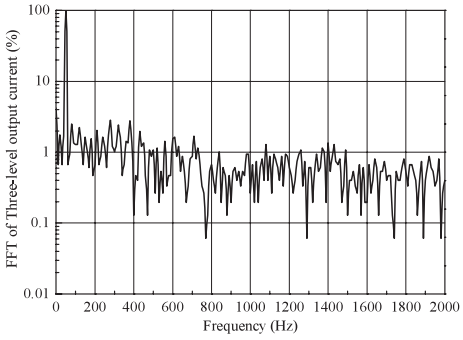


(d) Frequency spectra of load current.

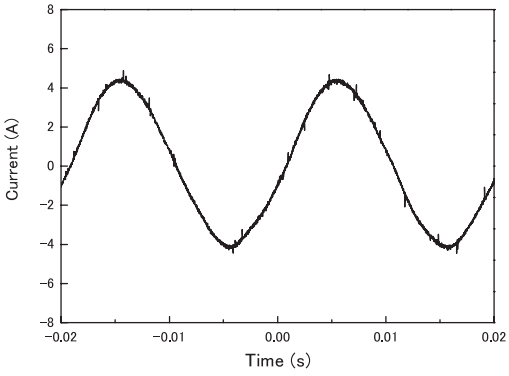
Fig. 9. Simulation result of proposed three-level CSI



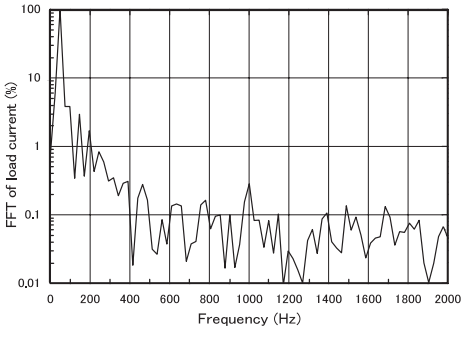
(a) Three level output current waveform.



(b) Frequency spectra of three-level output current



(c) Load current waveform.



(d) Frequency spectra of load current.

Fig. 10. Experimental result of proposed three-level CSI

small distortion (THD = 0.67%). Figure 11 shows the current waveforms flowing through the input inductor 1 and the input inductor 2. The results proves that the balancing of the input inductor currents is achieved by using the proposed current control system. Due to inherent nature of the circuit, the current ripple of the input inductors is directly transferred to the load. Figure 12 shows the PWM current synthesized by the sinusoidal PWM and the current flowing through the blocking diode of the chopper. Due to synchronized switching time between the chopper part and the inverter part, the on-state of Q1 does not distort the PWM current controlled by the sinusoidal PWM. Furthermore, Fig. 13 shows the harmonic profile of the three-level output current for different output current and load conditions.

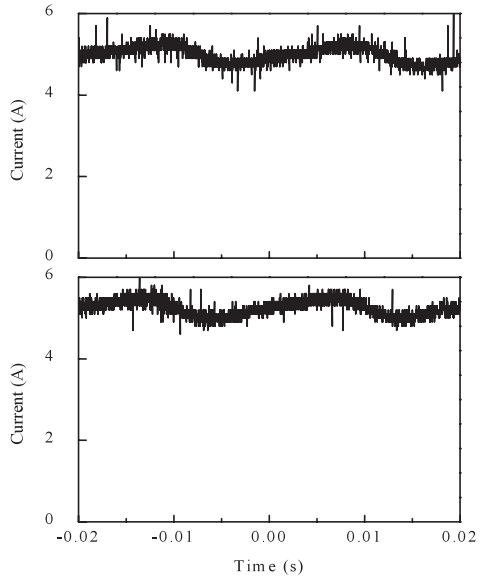


Fig. 11. Input inductor current waveforms

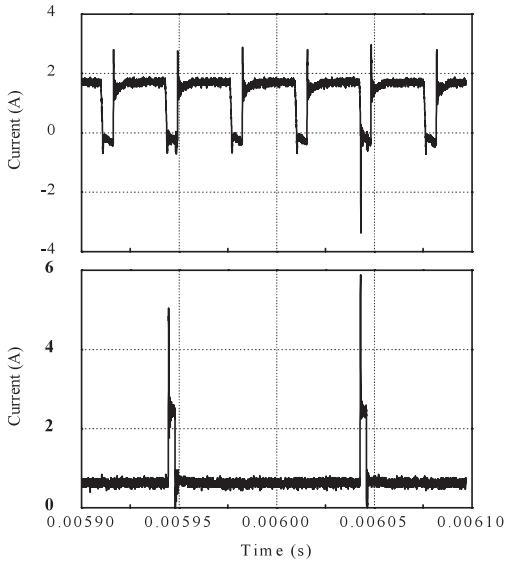


Fig. 12. Inverter PWM output current and blocking diode current

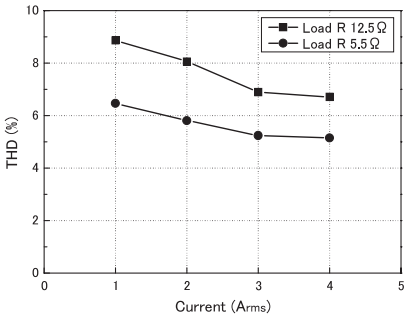


Fig. 13. Relationship between inverter output current and its THD

5. Conclusion

In this paper, a three-level current-source inverter with a full common-source topology at both of the chopper part and inverter part has been examined through computer simulations and experimental tests. Using this new current source inverter topology, the number of the gate drive power supplies has dramatically been reduced to only a single to drive all power switching devices used in the power circuit. By applying the proposed technique to a prototype inverter, excellent three-level current waveform as well as a proper operation has been confirmed in experimental tests, which proves feasibility of the proposed approach.

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References

(1) P.G. Barbosa, H.A.C. Braga, M.C. Barbosa, and E.C. Teixeria: "Boost Current Multilevel Inverter and Its Application on Single Phase Grid Connected Photovoltaic System", *IEEE Transaction on Power Electronic*, Vol.21, No.4, pp.1116–1124 (2006-7)

(2) S.B. Kjaer, J.K. Pedersen, and F. Blaajerg: "A Review of Single Phase Grid Connected Inverters for Photovoltaic Modules", *IEEE Transaction on Industry Application*, Vol.41, No.5, pp.1292–1306 (2005-9/10)

(3) J. Rodiguez, J.S. Lai, and F.Z. Peng: "Multilevel Inverter: A Survey of Topologies, Controls, and Application", *IEEE Transaction on Industrial Electronics*", Vol.49, No.4, pp.724–738 (2002-8)

(4) Y. Huang, F.Z. Peng, J. Wang, and D. Yoo: "Survey of the Power Conditioning System for PV Power Generation", *Power Electronics Specialist Conference*, pp.1–6 (2006)

(5) F.L.M. Antunes, A.C. Braga, and I. Barbi: "Application of a Generalized Current Multilevel Cell to Current Source Inverters", *IEEE Transaction on Power Electronic*, Vol.46, No.1, pp.31–38 (1999-2)

(6) K. Iwaya and T. Noguchi: "Novel Current Source Multilevel Inverter Driven by Single Gate Drive Power Supply", *IEEJ Trans. IA*, Vol.126, No.1, pp.10–16 (2006)

(7) T. Noguchi, S. Togashi, and R. Nakamoto: "Short Current Pulse Based Maximum Power Point Tracking Method for Multiple Photovoltaic and Converter Module System", *IEEE Transaction on Industrial Electronics*, Vol.49, No.1, pp.217–223 (2002-2)

(8) N. Mutoh, M. Ohno, and T. Inoue: "A Method for MPPT Control while Searching for Parameters Corresponding to Weather Conditions for PV Generation Systems", *IEEE Transaction on Industrial Electronics*, Vol.53, No.4, pp.1055–1065 (2006-8)

(9) Y. Xue, L. Chang, S.B. Kjaer, J. Bordonau, and T. Shimizu: "Topologies of Single Phase Inverter for Small Distributed Power Generators: An Overview", *IEEE Transaction on Power Electronic*, Vol.19, No.5, pp.1305–1314 (2004-9)

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