Generalized Multilevel Current-Source PWM Inverter with No-Isolated Switching Devices

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Abstract The paper proposes a generalized circuit configuration of a new multilevel current-source inverter (CSI) with no-isolated switching devices. In this new multilevel inverter topology, all of the power-switches in the inverter are connected on a common-potential level. Hence, all of the power switches only need a single gate drive power supply without using isolated power supplies or conventional bootstrap techniques. This key feature is still valid even if the number of the power switches increases due to the higher number of the output current waveform levels. As a result, complexity of the gate drive circuit can be remarkably moderated. In addition, the multilevel CSI circuit is capable to operate at high switching frequency if required, because all of the power switches are connected on the common potential level. Five-level PWM inverter configuration, including its chopper circuit as DC current-power source circuits using small input inductors, is verified through computer simulations and experimental tests. The results show feasibility of the proposed topology with reducing the circuit complexity and physical size of the multilevel CSIs.

Keywords-current-source inverter; common-emitter; multilevel; gate drive circuit

1. Introduction

The fast continuing development of power devices working at high switching frequencies for medium and high power applications such as metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs) has improved the power converter performance. In some high switching frequency applications, SiC (Silicon Carbide) based power MOSFETs and JFETs are very promising as next-generation power switching devices because their maximum voltage ratings and switching speeds can be about ten times of the conventional Si based devices. In addition, the ON-state resistance of SiC-MOSFETs will be reduced down to 1/500 of the currently available devices and their operating temperature can be over 300 °C, which is considerably effective to improve efficiency and power density of the power converters.

Development of high-performance semiconductor switches also increases the research interest in high power converters such as multilevel inverters because they have capability to output higher output power with low-voltage rating devices and less distorted output waveforms compared with the conventional two-level inverters. The multilevel inverter topologies can generally be classified into voltage source inverters (VSI) and its dual, i.e., current source inverters (CSI). The VSI has a DC voltage power source and generates AC voltage waveforms to the load, while the CSI delivers AC current waveforms from a DC current power source. The latter features capability of short-circuit protection because of its high impedance DC power source, but requires protection against an open-circuit to guarantee continuity of the current.

A large number of the power semiconductor switches in the multilevel inverter circuit increases circuit complexity such as control and gate drive circuits. In a high speed switching application, serious EMI and dV/dt problems cannot be ignored, especially high-frequency conductive noise currents in the gate driving circuits. Moreover, a bulky inductor used to obtain a smooth DC current and discrete diodes connected in series with the power switches are some drawbacks associated with the CSI topology, which often degrades its efficiency. However recently, the series diode might not be necessary because new IGBTs having reverse-blocking capability (reverse-blocking IGBTs) are emerging.

In order to address some problems such as dV/dt, inductor size, complexity of the gate drive-circuits and the control circuits of the multilevel CSI circuit, a new innovative solution is mandatory to make the multilevel CSI topology more attractive and popular. In this paper, a new generalized structure of the multilevel CSI circuit, where all of the power switches are connected on a common-emitter potential level, is presented. Using this multilevel inverter topology, the number of the gate drive power supplies for the power switches can dramatically be reduced to only a single to drive all the power switches without any isolated power supplies nor conventional bootstrap circuits. This significant feature is also valid even the number of the power switches increases to generate the higher level number of the output current waveform. In addition, the circuit can overcome the dV/dt problem in the inverter; because all the switches are connected on the identical potential level. In order to reduce the inductor size for the current source generation, a high-frequency chopper circuit generating a smooth DC input current for the CSI is also presented with its simple controller.

The operating performance of the proposed multilevel CSI is examined and validated through some computer simulations. Furthermore, a laboratory experimental prototype of a five-level CSI circuit was set up to verify the proposed new multilevel CSI topology, using the power MOSFETs with series blocking diodes.

2. Circuit Configuration and Principle Operation

2.1. Operation Principle of Inverter Circuit

Figure 1 shows a circuit configuration of a three-level CSI proposed in the authors' previous research. All of the power switches Q1, Q2, Q3 and Q4 are connected on a common-emitter line. Table 1 lists its switching states of this three-level CSI for three-level output current waveform generation +I, 0 and –I current-levels. In addition, Fig. 2 shows another basic circuit configuration of a two-level CSI-module

of which power switches Q5 and Q6 are also connected on a common potential point. Its switching states are presented in Table 2. The newly proposed configuration of the multilevel CSI can be obtained by connecting the former three-level CSI as a main inverter circuit, with a single or some two-level CSI-modules via connecting diodes as shown in a generalized circuit of the proposed CSI in Fig. 3.

A unique point of the proposed multilevel CSI circuit is that all of the power switches are connected on a common-emitter or a common-potential point. This condition is still valid even the number of the power switches increases to generate the higher level number of the output current waveform. The relation between the level number of the CSI output current waveform and the number of the two-level CSI modules can be obtained from the equation below:

$$M=3+2n, \quad (1)$$

where *M* is the level number of the output current and *n* is the number of two-level CSI-modules. Figure 4 and 5 show a configuration of the five-level CSI and its principle operation waveform, respectively. In this example, all of the DC current sources are assumed to have the identical current amplitude, i.e., $I_1=I_2=I_3=I_4=I$.

Using this new multilevel CSI topology, several advantages can be obtained as follows:

1) Using this circuit topology, the number of the gate drive power supplies can be reduced drastically; hence, it can reduce the circuit component and circuit complexity of the gate drive circuits, such as isolation transformers; in case of isolated power supplies are used for each power switch; or capacitors; in case of bootstrap technique is applied.
2) All power switches are connected at the identical reference potential; hence it can eliminate the dV/dt problem during the switching operation. Therefore, the inverter can be operated at a high switching frequency in order to obtain better quality of the inverter output current by pushing harmonic components to a higher frequency range.
3) A simple and modular structure. The inverter circuit is composed of multiple units of an identical two-level CSI, which leads to cost reduction in manufacturing process.
4) A single DC power source. The level of the output current can be increased easily by connecting some two-level CSI modules with only a single DC power source.

Table 1 Switching states of three-level CSI

Q_1	Q_2	Q_3	Q_4	Output
0	0	1	1	+I
1	0	0	1	0
1	1	0	0	-I

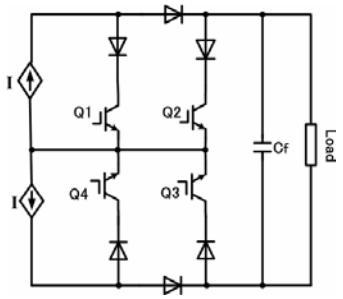


Fig. 1. Fundamental three-level CSI

Table 2 Switching states of two-level CSI

Q_5	Q_6	Output
0	1	+I
1	0	-I

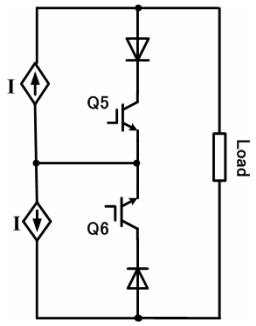


Fig. 2. Two-level CSI module

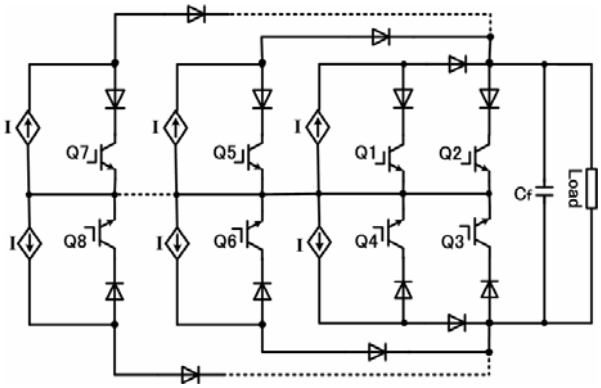


Fig. 3. Generalized configuration of proposed multilevel CSI

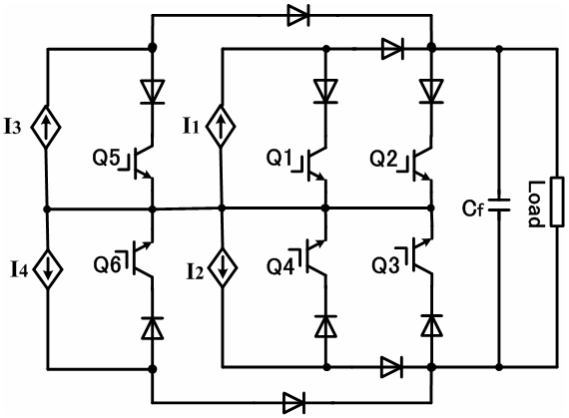


Fig. 4. Five-level CSI circuit ($I_1=I_2=I_3=I_4=I$)

Table 3 Switching states of five-level CSI

Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Output
0	0	1	1	1	1	+I
0	0	1	1	0	1	+2I
1	0	0	1	1	1	0
1	1	0	0	1	1	-I
1	1	0	0	1	0	-2I

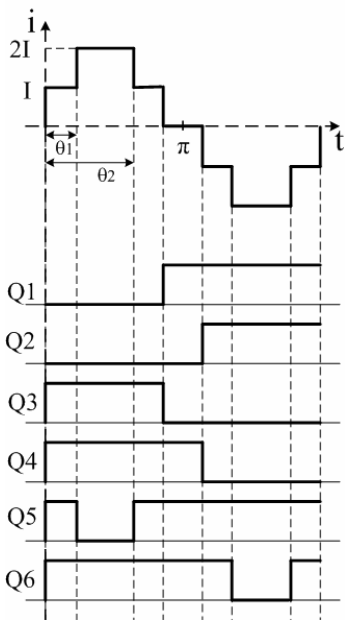
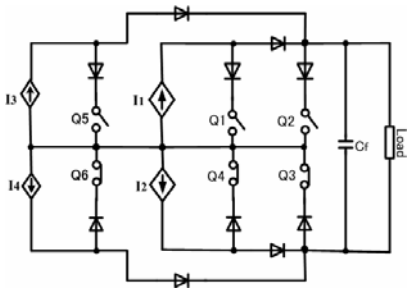


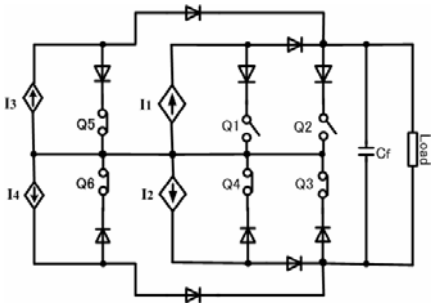
Fig. 5. Five-level current waveform generation

The switching state combinations required to generate a five-level current waveform are listed in Table 3 and illustrated in Fig. 6(a) to (e). The required five-level output current (+2I, +I, 0, -I and -2I current-levels) are generated as follows:

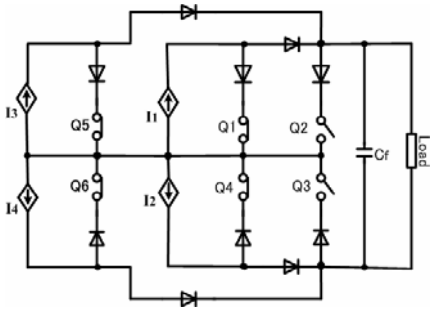
1) Current level +2I: Q1, Q2 and Q5 are turned off, while Q3 is turned on, making the currents I1 and I3 flow to the load. Q4 and Q6 are turned on, making the current circulation paths for other two DC current sources (I2, I4).
2) Current level +I: Q1 and Q2 are turned off, while Q3 is turned on, making the current I1 flows to the load. Q4, Q5 and Q6 are turned on, making the current circulation paths for other three DC current sources input inductor current (I2, I3, I4).
3) Current level 0: Q1, Q4, Q5 and Q6 are turned on, and Q2 and Q3 are turned off making the current loops for every DC current source. No current flows to the load.
4) Current level -I: Q3 and Q4 are turned off, while Q2 is turned on, making the current I2 flows to the load. Q1, Q5 and Q6 are turned on, making the current path for other three DC current sources (I1, I3, I4).
5) Current level -2I: Q3, Q4 and Q6 are turned off, while Q2 is turned on, making the currents I2 and I4 flow to the load. Q1 and Q5 are turned on, making the current paths for other two DC current sources (I1, I3).



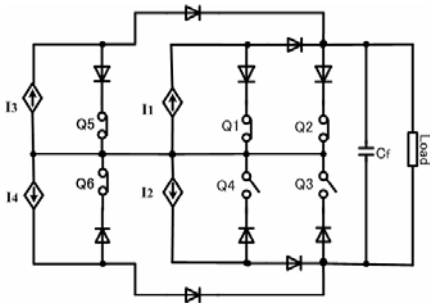
(a) Current +2I



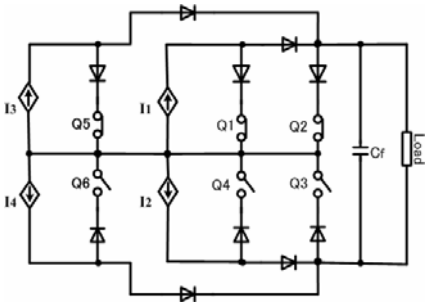
(b) Current +I



(c) Current 0



(d) Current -I



(e) Current -2I

Fig. 6. Switching modes for five-level current generation ($I_1=I_2=I_3=I_4=I$)

2.2. DC Current-Source Circuit

In this multilevel CSI circuit, the DC current sources are required, which are obtained by employing chopper circuits with small inductors connected with each CSI module working as a DC current supply. The chopper circuit consists of two controlled switches controlling a pair of the DC currents flowing through two smoothing inductors. Two free-wheeling diodes are used to keep continuous currents flowing through the inductors. Figure 7 shows the two-level CSI module with chopper circuit as the DC current supplies.

The controller diagram of the chopper circuit for DC current generation is presented in Fig. 8. Proportional integral (PI) regulators are independently applied to control two of the currents flowing through the smoothing inductors L1 and L2, which determine the amplitude of the PWM output current waveform (Ipwm) simultaneously. Making the inductor currents (I_{L1} and I_{L2}) follow their reference current (Iref) is the objective of this current regulator. The switching gate signals of the chopper switches are generated by comparing the error signal of the detected steady state currents flowing through the input inductors I_{L1} and I_{L2}, and a triangular waveform after passing through the PI regulator. This signal is used to control the duty cycles of the chopper switches to obtain balanced and stable DC currents I_{L1} and I_{L2}. This control circuit is similar for all of the chopper circuits accompanying the two-level CSI module functioning as the DC current supplies; thus this approach effectively makes the controller much simpler. By connecting more and more two-level CSI modules, the higher level number of the output current waveform with smaller current rating switching devices and smaller distortion of the output current waveform can be obtained.

Figure 9 shows a circuit configuration of a five-level CSI including the chopper circuits as DC current sources. The power circuit consists of a three-level CSI as a main circuit connected with a two-level CSI module. Only a single DC power source is required to obtain the four DC current sources for the CSI.

2.3. PWM Modulation Strategy

In order to obtain a better output current waveform, a pulse width modulation (PWM) technique is applied, instead of a staircase waveform operation. Staircase waveform can easily be obtained at the fundamental switching frequency, so switching losses can be negligibly low. However more distortion of the output waveform is generated and a larger filter is needed.

In this paper, a level-shifted multi-carrier based sinusoidal PWM technique is employed to generate the gate signals for the CSI power switches to obtain the PWM current waveforms as shown in Fig. 10. All carrier waveforms are in phase with the identical frequency. The frequency of the modulated signal (a reference sinusoidal waveform) determines the fundamental frequency of the output current waveform, while the frequency of triangular carrier waves gives the switching frequency of the CSI power switches. An *M*-level output current waveform using this modulation requires *(M-1)* triangular carriers with the same frequency.

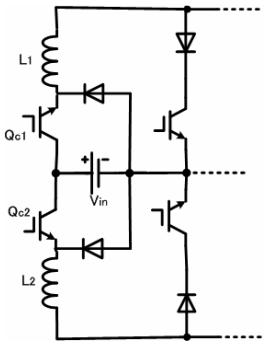


Fig. 7. Two-level CSI module with chopper circuit

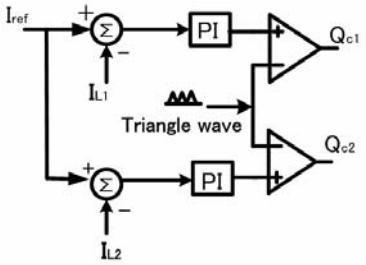


Fig. 8. Controller diagram of chopper circuit

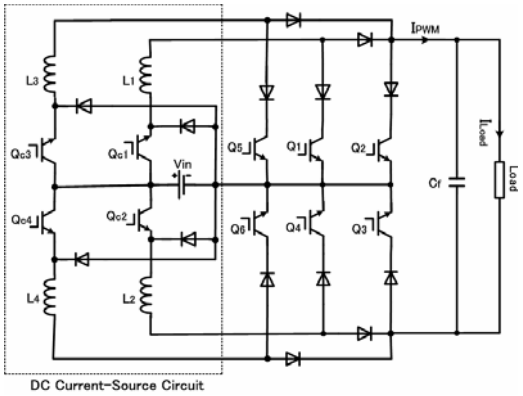


Fig. 9. Simulation and experimental test circuit of five-level CSI

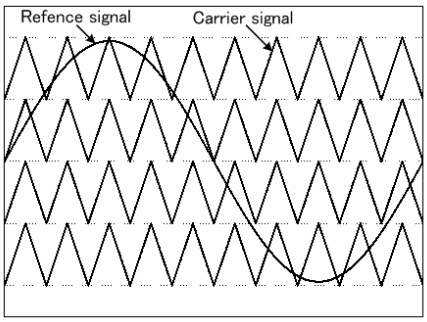


Fig. 10. Multi-carrier based sinusoidal PWM

Table 4 Test parameters

Smoothing inductors of chopper	600 μH
Power source voltage	DC 160 V
Switching frequency	30 kHz
Filter capacitor of load	5 μF
Load	R= 6 Ω , L= 1.2 mH

3. Computer Simulation Results

In order to analyze and to test the proposed topology, computer simulations are conducted by using a PSIM software. This section presents an example the computer simulation results of the proposed five-level CSI. The simulation parameters are shown in Table 4. The five-level inverter circuit configuration shown in Fig. 9 is tested with a single DC power source. Figure 11 shows an overall controller diagram of the five-level CSI including its chopper and inverter circuit controller.

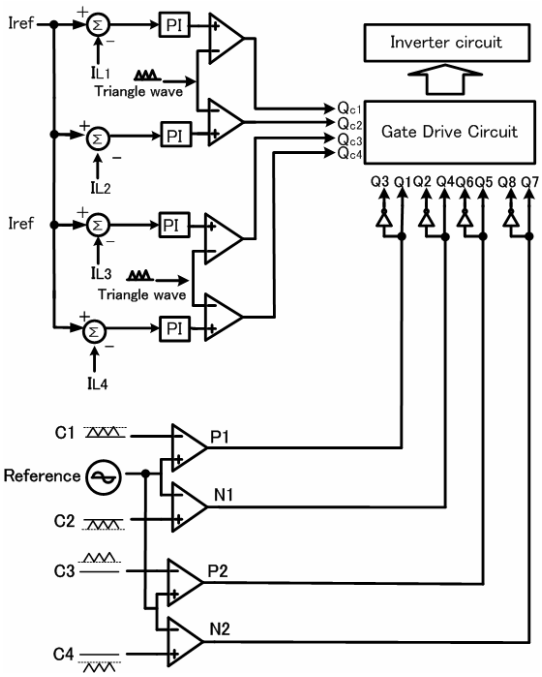


Fig. 11. Controller diagram of five-level CSI

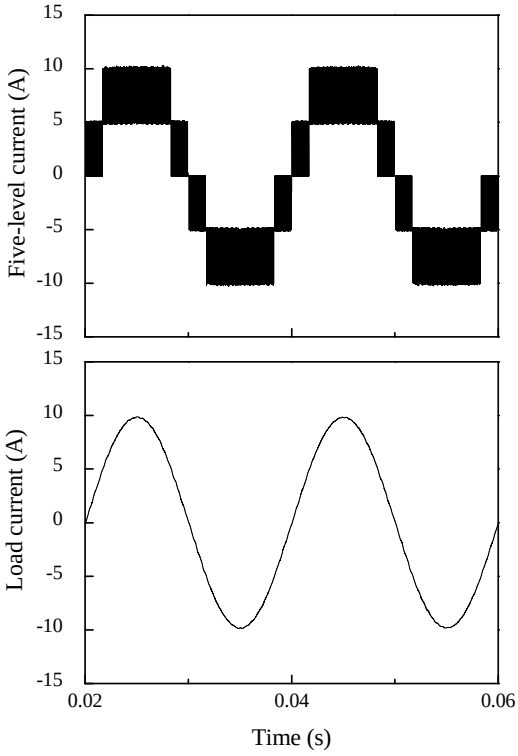
Figures 12(a) and (b) present the computer simulation results of five-level current, the load current and the DC power source currents for the five-level CSI. The amplitude of the DC current sources are well balanced for all smoothing inductors (I_{L1}, I_{L2}, I_{L3} and I_{L4}), which correspond to a half of the peak level of the five-level output current waveform. It is confirmed that the five-level CSI generates the five-level output current perfectly.

4. Experimental Test Results

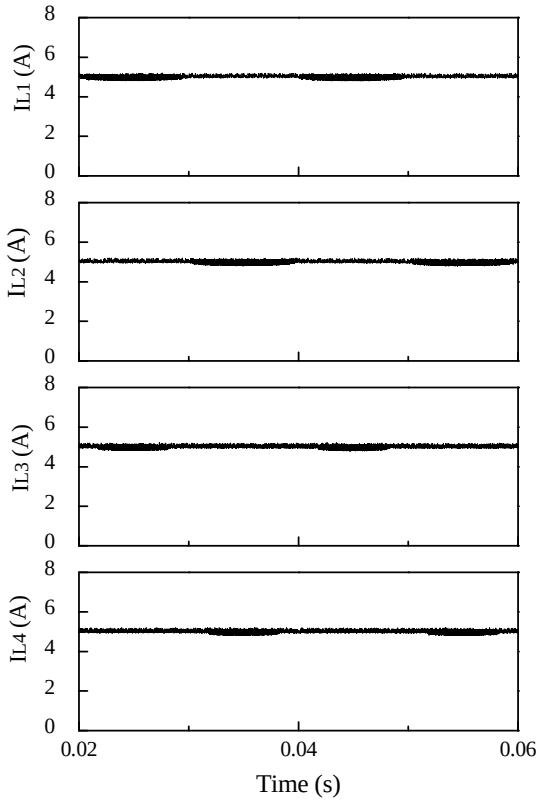
In order to verify feasibility of the proposed multilevel CSI configuration experimentally, laboratory prototypes of the five-level and seven-level CSI were constructed with 300-V, 30-A power MOSFETs (FK30SM-6) and 1200-V, 16-A fast recovery diodes (HFA16PB120). The experimental circuit specifications are identical with the computer simulation parameters as listed in Table 4.

Figures 13(a) and (b) show the resultant experimental waveforms of the five-level CSI showing the steady state five-level output current, the load current and the DC current source waveforms obtained from the chopper circuits. The inverter works properly generating a five-level output current waveform. As can be seen in the figure, a low distorted sinusoidal load current waveform is also obtained after filtering. All of the experimental waveforms agree with the previous computer simulation results.

Figure 14 shows efficiency characteristics of the three-level, five-level and seven-level CSIs. As can be seen, the proposed strategy can improve the overall efficiency of multilevel CSI effectively. The efficiency is low in a light load condition which is caused by conduction losses of the inductors and switching devices becoming relatively dominant against the load power. However, the efficiency increases as the load becomes heavier, and the maximum efficiency of the seven-level CSI prototype was confirmed to be 93.1 %.

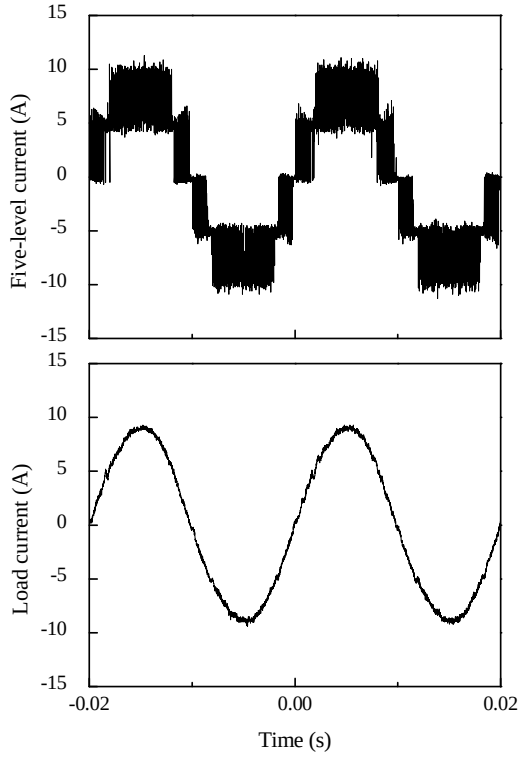


(a) Five-level and load currents

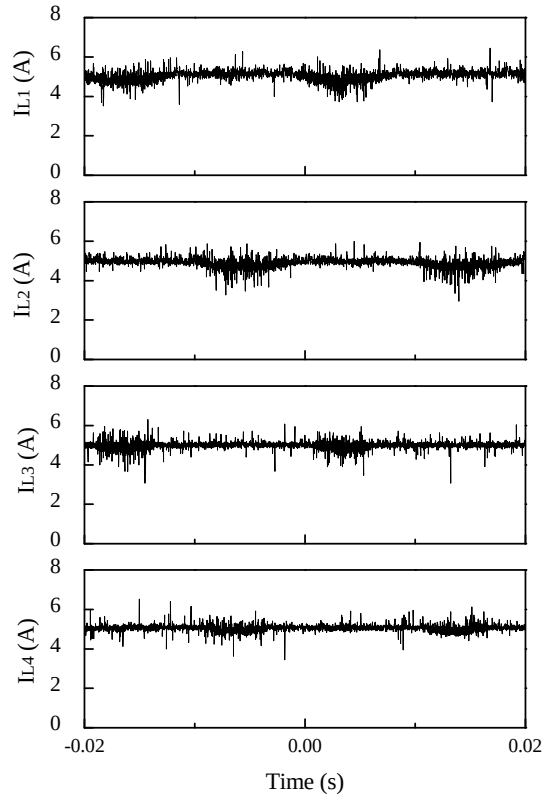


(b) Waveforms of DC current sources

Fig. 12. Simulation waveforms



(a) Five-level and load currents



(b) Waveforms of DC current sources

Fig. 13. Experimental waveforms

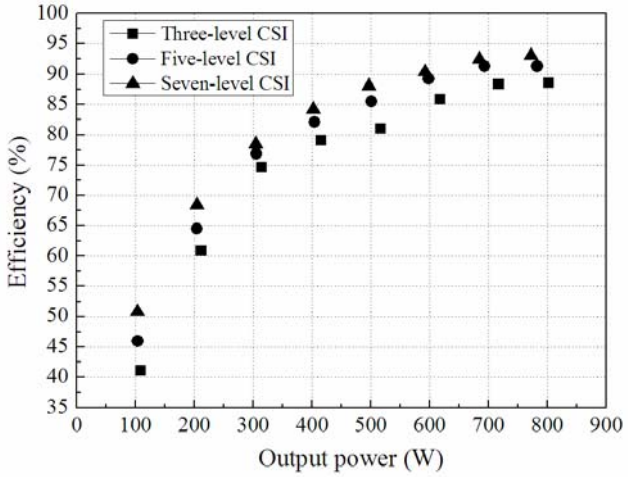


Fig. 14. Efficiency characteristics of proposed multi-level CSIs

5. Conclusion

In this paper a new generalized configuration of a multilevel CSI has been proposed and its validity has been verified using computer simulations and an experimental prototype. The multilevel inverter topology can drastically reduce complexity of the gate drive circuits and the control circuit in the multilevel CSI. This remarkable feature never fades away even if the number of the power switches is increased to achieve higher level number of the output current waveform. Chopper circuits working as DC current sources are also discussed which are able to reduce the input inductor size down to micro-H order.

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