Novel H-Bridge Multilevel Current-Source PWM Inverter with Inductor-Cells

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***Abstract*--The paper proposes a new circuit configuration of multilevel current-source inverter (CSI). In this new topology, a basic H-Bridge CSI working as a main inverter is connected in parallel with inductor-cells operated as auxiliary circuits. The inductor cell is composed by four unidirectional power switches with an inductor across the cell circuit. The inductor-cells work generating the intermediate level currents to obtain a multilevel current waveform without additional external DC power sources. A simple PI controller is applied to control the intermediate level currents of multilevel output waveform. Five-level and nine-level PWM inverter configurations, with chopper based DC current source, are verified through computer simulations. Furthermore, an experimental prototype of a five-level CSI is setup and is tested. The results show that the proposed circuit works properly to generate the multilevel output current waveform with low harmonics distortion by using small inductors.**

Keywords-current-source inverter; H-bridge, inductor-cell; multilevel

I. INTRODUCTION

Recent development of high-performance semiconductor power switches such as MOSFETs and IGBTs increases the research interest in high power converters such as multilevel voltage source inverters (VSI) and its dual circuit, multilevel current source inverters (CSI). They have capability to deliver higher output power with lower dv/dt or lower di/dt and less distorted output waveforms resulting in reduction of EMI noise and size of output filter [1], [2].

In distributed generation application, as most renewable energy sources, such as photovoltaic system, deliver dc power, the generated power must be converted to ac power and is fed into the grid through a grid connected inverter [3], [4]. Various international standards, like IEEE-1547, IEEE-929 and EN-61000-3-2, impose requirements on the inverter's output power quality, such as harmonic currents and total harmonics distortion (THD) of the output current. Multilevel CSI is one of effective solutions to tackle such problem. Control of the grid connected CSI is comparatively simpler than its counterpart, VSI. A grid connected CSI can buffer the output from grid voltage fluctuation, generates a predetermined magnitude of current to the grid without ac current feedback loops, and can achieve a high power factor operation abilities [3]. Its output current is less affected by grid voltage, and it has inherent short circuit protection. Moreover, the discrete diodes connected in series with the power switches to obtain unidirectional power switches in CSI will be unnecessary because new reverse-blocking IGBTs are emerging [5].

Some topologies of multilevel CSIs have been proposed by researchers and engineers. A conventional method to generate the multilevel output waveforms is by paralleling some three-level H-Bridge CSIs as shown in Fig. 1 [6]-[8]. However, the requirement of many isolated DC current sources is a problem introduced by this configuration. Another topology of multilevel CSI is by applying multi-cell topology of CSI, which is the dual converter of flying capacitor multilevel VSI [9]-[11]. But this topology has drawback with its huge intermediate inductors and its control complexity for balancing control of the intermediate level currents. References [12] and [13] presented the common-emitter configuration (or "fish bone structure") of multilevel-CSI obtained by connecting two-level CSI modules with the three-level common-emitter CSI. This configuration has a great advantage because all of the power switches are connected at a common-emitter point. This topology needs only a single isolated gate drive circuit to drive all power switches of the inverter, hence the complexity of the gate drive circuits can be moderated.

This paper proposes a circuit configuration of a new multilevel CSI. In this new topology, a basic H-bridge CSI working as a main inverter circuit is connected in parallel with inductor-cells. The inductor-cells work generating the intermediate level currents of the output to obtain a multilevel current waveform without any additional external dc power sources. The operating performance of the proposed multilevel CSI is examined and tested through some computer simulations and experimentally.

II. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

A. Operation Principle of Proposed Multilevel CSI

Fig. 2 shows a configuration of proposed inductor-cell circuit composed by four unidirectional controlled power switches Q_{C1}, Q_{C2}, Q_{C3} and Q_{C4}, and an inductor Lc connected across the cell circuit. The newly proposed configuration of the multilevel CSI can be obtained by connecting the three-level H-Bridge CSI with a single or more inductor-cells as shown in a schematic diagram of the proposed multilevel CSI in Fig. 3. A five-level CSI configuration is obtained by connecting a single inductor-cell, a nine-level CSI configuration is achieved by connecting two inductor-cells in parallel with the main three-level H-bridge CSI, and so forth. The relation between the level number of the output current waveform (M) and the number of the inductor-cells (N) can be formulated as expressed by the equation below:

$$M = 2^{(N+1)} + 1. \quad (1)$$

Fig. 4 and 5 show the configurations of five-level and nine-level CSIs using the proposed strategy, respectively.

The inductor-cells work generating the intermediate level currents of a multilevel output waveform from the basic three-level current of H-bridge CSI. It utilizes the charging and discharging operation modes of the inductor. Fig. 6 shows the operation modes of the inductor-cell during a positive cycle operation of the five-level CSI. Charging operation mode of the inductor Lc is conducted when the switches Q_{C1} and Q_{C3}

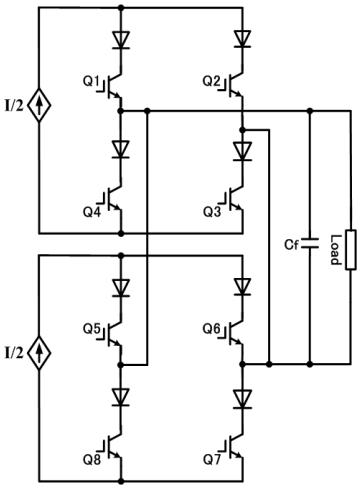


Fig. 1. Parallel H-Bridge five-level CSI

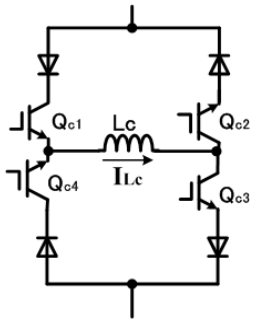


Fig. 2. Proposed inductor cell circuit

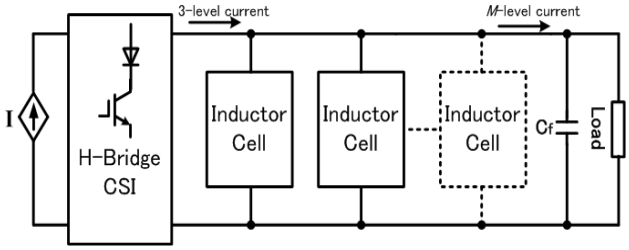


Fig. 3. Proposed configuration of multilevel CSI

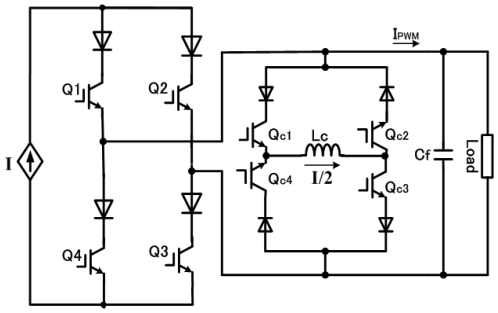


Fig. 4. Proposed five-level CSI

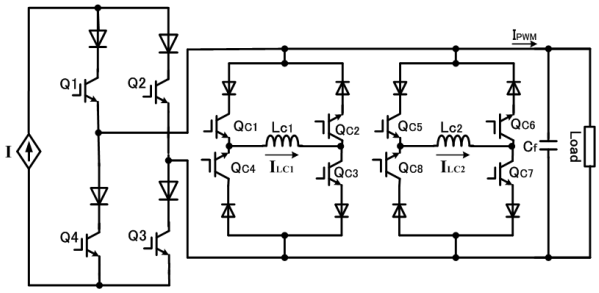
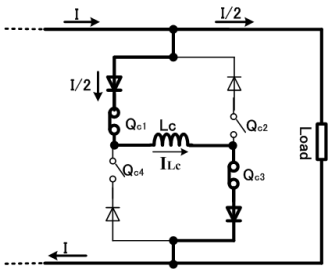
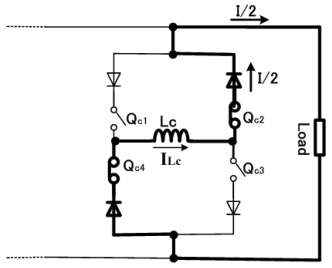


Fig. 5. Proposed nine-level CSI



(a) Charging mode of inductor-cell



(b) Discharging mode of inductor-cell

Fig. 6. Operation modes of inductor-cell

TABLE I. SWITCHING STATES OF FIVE LEVEL CSI

Q_1	Q_2	Q_3	Q_4	Q_{c1}	Q_{c2}	Q_{c3}	Q_{c4}	**Output**
1	0	1	0	1	1	0	0	+I
1	0	1	0	0	0	1	1	+I
1	0	1	0	1	0	1	0	+I/2
1	0	0	1	0	1	0	1	+I/2
1	0	0	1	1	1	0	0	0
1	0	0	1	0	0	1	1	0
0	1	0	1	0	1	0	1	-I/2
1	0	0	1	1	0	1	0	-I/2
0	1	0	1	0	0	1	1	-I
0	1	0	1	1	1	0	0	-I

are turned on, while Q_{C2} and Q_{C4} are turned off. A current I_{Lc}=I/2 flows through the power switches Q_{C1} and Q_{C3} which energizes the inductor L_c. Discharging operation mode is achieved by turning on the switches Q_{C2} and Q_{C4} and by turning off Q_{C1} and Q_{C3}. The stored energy in the inductor is discharged to the load as a current I/2. Similar operation modes occurred for the negative cycle of output current waveform. For *M*-level CSI, if the DC current-source of the main H-bridge CSI is assumed to have an amplitude I, the current flowing through the N^{th} inductor cell $I_{LC(i)}$ is expressed as

$$I_{Lc(i)} = \frac{I}{2^i}, \text{ i=1, 2,… N.} \quad (2)$$

The output current levels of the five-level CSI are +I, +I/2, 0, -I/2, and -I current levels. For nine-level CSI, the outputs are +I, +3I/4, +I/2, +I/4, 0, -I/4, -I/2, -3I/4, and -I current levels. TABLE I lists the switching states of the proposed five-level CSI.

The five output current levels +I, +I/2, 0, -I/2 and -I of five-level CSI are generated as follows:

1) Current level +I
   Q1, Q3, Q_{C1} and Q_{C2} are turned on, while Q2, Q4, Q_{C3} and Q_{C4} are turned off, making the current +I flow to the load;
2) Current level +I/2
   Charging mode: Q1, Q3, Q_{C1} and Q_{C3} are turned on, while Q2, Q4, Q_{C2} and Q_{C4} are turned off, making the currents of +I/2 flow to the load and to the inductor-cell at the same time. The inductor-cell is energized in the charging mode.
   Discharging mode: Q1, Q4, Q_{C2} and Q_{C4} are turned on, while Q2, Q3, Q_{C1} and Q_{C3} are turned off, making the stored energy in the inductor be released to the load as a current +I/2. The inductor-cell is in the discharging mode;
3) Null current level
   Q1, Q4, Q_{C1} and Q_{C2} are turned on, while Q2, Q3 Q_{C3} and Q_{C4} are turned off, making the current loop for input dc current source and inductor-cell current. No current flows to the load;
4) Current level –I/2
   Charging mode: Q2, Q4, Q_{C2} and Q_{C4} are turned on, while Q1, Q3, Q_{C1} and Q_{C3} are turned off, making the current of –I/2 flow to the load, and the inductor-cell current is kept at the constant value of I/2. The inductor-cell works in the charging mode even though the negative cycle of the output.
   Discharging mode: Q2, Q3, Q_{C1} and Q_{C3} are turned on, while Q1, Q4, Q_{C2} and Q_{C4} are turned off, causing the stored energy in the inductor is discharged to the load as a current -I/2. The inductor cell is in the discharging mode; and
5) Current level –I
   Q2, Q4, Q_{C3} and Q_{C4} are turned on, while Q1, Q3, Q_{C1} and Q_{C2} are turned off, making the current -I flow to the load.

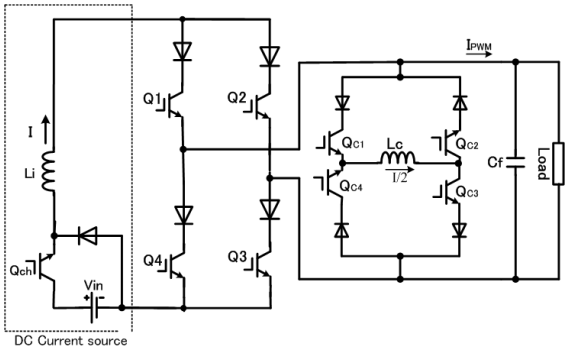


Fig. 7. Five-level CSI with chopper based DC current source

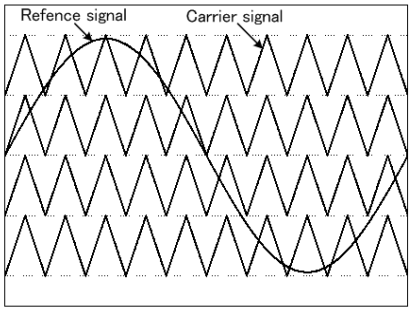


Fig. 8. Multi-carrier based sinusoidal PWM

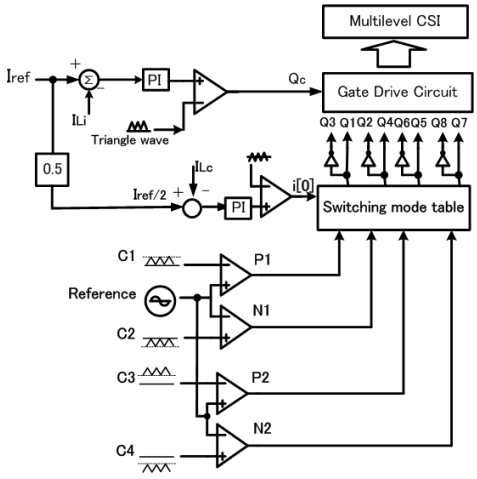


Fig. 9. Control diagram of proposed five-level CSI

TABLE II. TEST PARAMETERS

Smoothing inductor and inductor cell	1 mH and 5 mH
Power source voltage	160 V
Inverter switching frequency	22 kHz
Filter capacitor C*f*	5 μF
Load	R = 6.2 Ω , L =1.2 mH
Output current frequency	60 Hz

B. DC Current Source

In the proposed multilevel CSI, the dc current source is indispensable. In order to test the proposed multilevel CSI, the dc current source is obtained by employing a chopper with a smoothing inductor connected with the main three-level H-bridge inverter. The chopper consists of a controlled switch that regulates the dc current flowing through the smoothing inductor Li. A free-wheeling diode is used to keep continuous current flowing through the smoothing inductor. The chopper works as a regulated dc current source. Fig. 7 shows the five-level CSI configuration with the chopper based dc current source. The power source (V_{in}) may be batteries, PV modules, a fuel-cell or a rectifier.

A simple proportional integral (PI) regulator is applied to control the dc current flowing through the smoothing inductor, which determines the amplitude of the PWM output current waveform I_{pwm} simultaneously. Making the inductor current follow the reference current is an objective of this current regulator. The switching gate signals of the chopper switch (Q_c) is generated by comparing the error signal of the detected steady state inductor current, and a triangular waveform after passing through the PI regulator. This signal is used to control the duty cycles of the chopper switch to obtain a stable dc current waveform even a small smoothing inductor is used.

C. PWM Technique and Inductor-Cell Control

In order to achieve a low distortion of the output current waveform, a pulse width modulation (PWM) technique is applied. In this paper, a level-shifted multi-carrier based sinusoidal PWM technique is employed to generate gate signals for the CSI power switches and to obtain the PWM current waveforms as shown in Fig. 8. A schematic control diagram including the current controller of the chopper and the inductor-cell for the five-level CSI is shown in Fig. 9.

The control circuit of the inductor-cell functions to control the operation modes, i.e. charging and discharging modes, of the inductor-cell (Lc). The current flowing through the inductor-cell I_{Lc} is kept constant. It generates the intermediate level currents based on the output waveform of the H-Bridge CSI. A PI regulator is applied to zero the error between the detected current flowing through the inductor-cell and the reference current which is half of the main dc current to obtain stable and balanced intermediate level currents. The output of the PI regulator is modulated by a triangular carrier to generate the control signal i[0] determining the operation modes of the inductor-cell. The frequency of the triangular carrier waveform determines the switching frequency of the inductor-cell's power switches which also regulates the charging and the discharging modes of the inductor-cell. In case of the nine-level CSI, the control circuit of the second inductor-cell is similar to the first inductor-cell mentioned above. The difference is only the reference value of the second inductor-cell current I_{Lc2}, which is quarter of the main dc current-source amplitude. Therefore, for *M* level CSI, if the dc current source of the main H-bridge CSI is assumed to have amplitude I, the current flowing through the N^{th} inductor-cell I_{Lc} is expressed as in (2).

III. SIMULATION RESULTS

In order to test the proper operation of the proposed multilevel CSI topology, a five-level and a nine-level CSI configurations as shown in Fig. 4 and 5 with chopper based dc current source were tested by using computer simulation with a PSIM software. The test parameters are listed in TABLE II. Fig. 10(a) shows the computer simulation result of the proposed five-level CSI, where the five-level and the load current waveforms are presented. Fig. 10(b) shows the dc input current and the inductor-cell current waveforms. Fig. 11(a) shows another computer simulation result of proposed nine-level CSI showing the nine-level and the load current waveforms. Fig. 11(b) shows the dc input current, the first (I_{Lc1}) and the second inductor-cell (I_{Lc2}) current waveforms of the nine-level CSI. As can be seen in the result, the amplitudes of the first and the second inductor-cell currents are properly driven to be 50% and 25% of the 8-A dc input current, respectively.

IV. EXPERIMENTAL TEST RESULTS

In order to verify and to prove feasibility of the proposed multilevel CSI configuration, a laboratory prototype of the five-level CSI was constructed with IXFK90N30 power MOSFETs in series with DSEI120-06A fast recovery diodes. The implemented circuit specifications are identical with the computer simulation parameters in TABLE II.

Fig. 12(a) shows the experimental waveforms of the five-level CSI, i.e., an 8-A, 60-Hz five-level PWM output current and a load current waveforms with modulation index 0.9. Fig. 12(b) shows the current waveforms flowing through the smoothing inductor and inductor-cell. The amplitude of the inductor-cell current is confirmed to be half of the 8-A dc input current. The inverter worked properly generating a five-level output current waveform. In addition, a low distorted sinusoidal load current waveform is also obtained after filtering by a small 5-μF filter capacitor. All of the experimental waveforms agree with those of the computer simulation results. The measured THD value of the five-level PWM current is 2.93%.

V. CONCLUSIONS

In this paper a new configuration of multilevel CSI, which employs inductor-cells as auxiliary circuits has been proposed. The inductor-cells are connected in parallel with the main H-bridge CSI to generate multilevel output current waveforms without additional external dc power sources. A chopper based dc current source is also introduced in order to reduce the size

of the smoothing inductor. The validity of the proposed topology has been verified through computer simulations and experimentally. The simulation and experimental results show that using the proposed multilevel CSI a low distortion of output current can be obtained by using small inductors.

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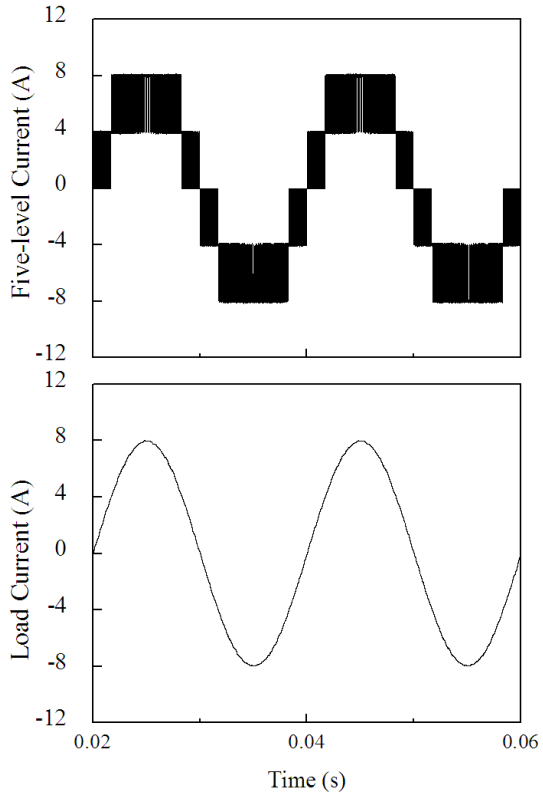
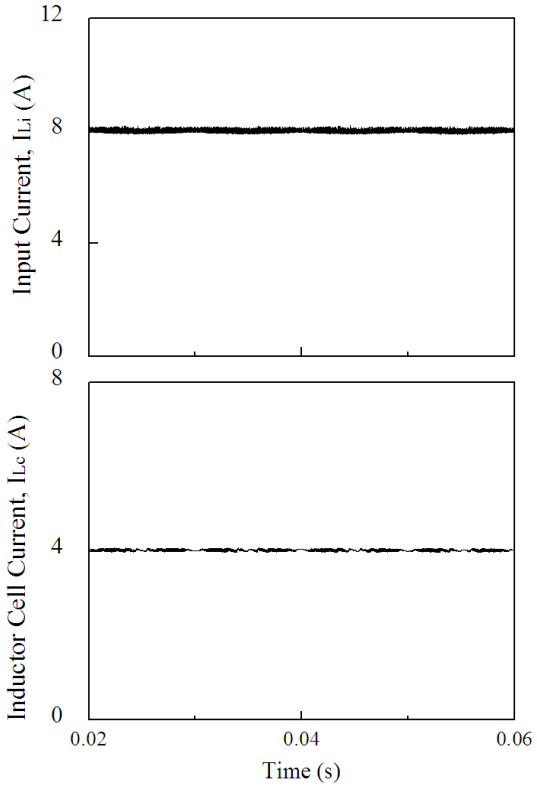
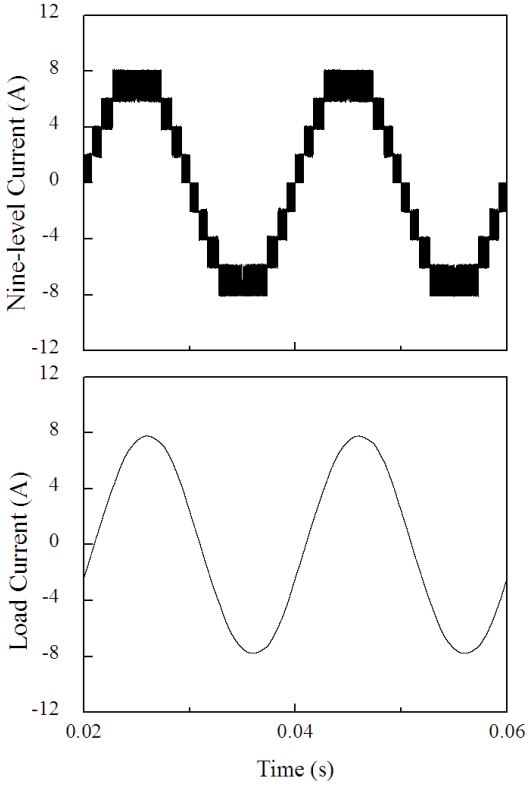


(a) Five-level and load current waveforms

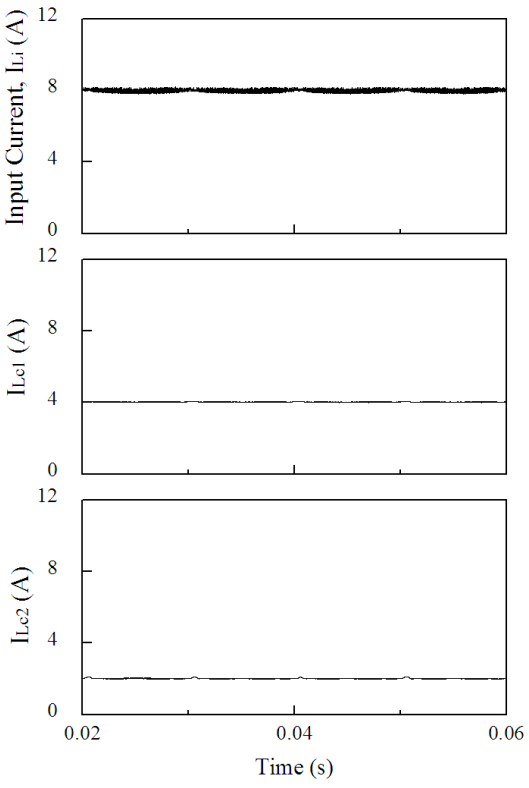


(b) Dc input current I_{Li} and inductor-cell current I_{Lc}

Fig. 10. Simulation result of the proposed five-level CSI

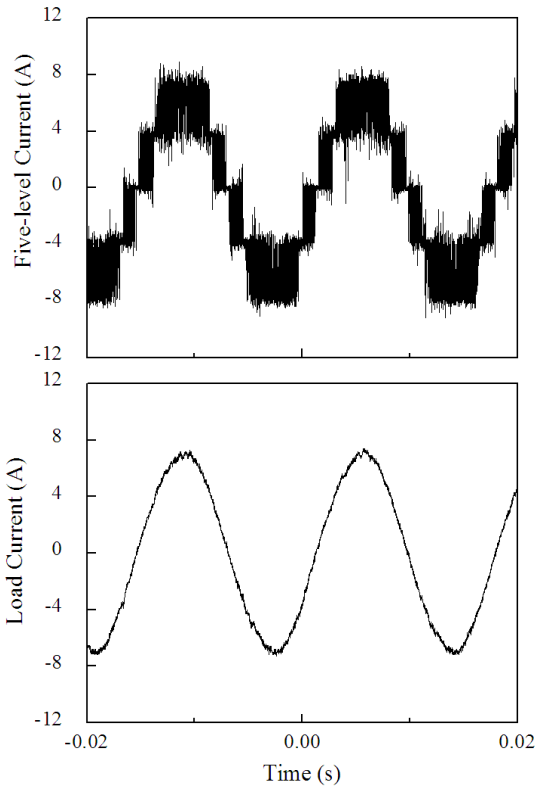


(a) Nine-level and load current waveforms

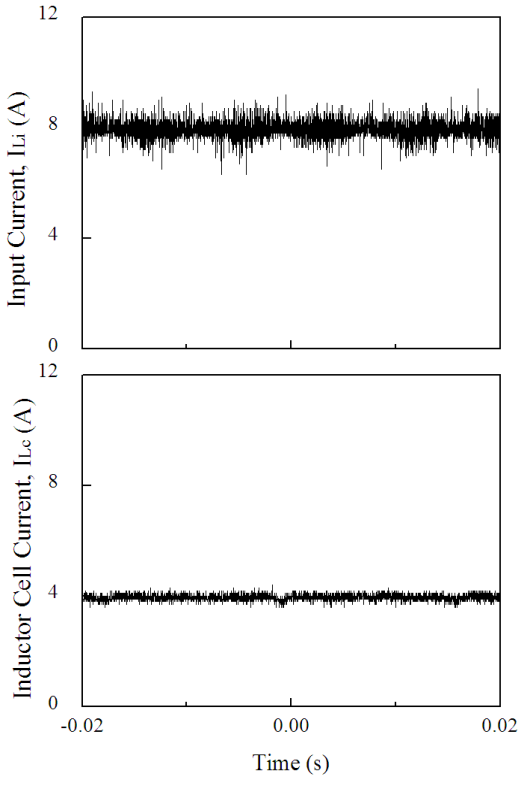


(b) Dc input current and inductor-cell current waveforms

Fig. 11. Simulation result of nine-level CSI



(a) Five-level and load current waveforms



(b) Dc input current and inductor-cell current waveforms

Fig. 12. Experimental test result of five-level CSI