High-Speed Switching Operation of MOSFETs Using Auxiliary Circuit Shorting Load

- Applications to Chopper and Half-Bridge Inverter and Their Operation Characteristics -

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Abstract— **This paper describes a high-speed switching technique of power MOSFETs applied to a chopper and a half-bridge inverter. The switching time must be shortened to operate power converters using the power MOSFETs at high-frequency, but parasitic output capacitance prevents the MOSFETs from turning off fast. In general, the turn-off time becomes longer as a load current is reduced because the reduced drain current takes a long time to charge the parasitic output capacitance. In the paper, a set of auxiliary switches and diodes in parallel with a load is proposed to reduce the turn-off time effectively. This additional auxiliary circuit makes a high-frequency drive of the power MOSFETs and switching-loss reduction of the power converter possible. It has been confirmed through experimental tests that the operational frequency range of the power converter expands to MHz-order and that the power conversion efficiency is effectively improved in a low-load range by employing the proposed technique.**

Keywords-component; MOSFET, high-speed switching, turn-off, auxiliary circuit, chopper, half-bridge inverter

I. INTRODUCTION

In recent years, great attention has been paid on next-generation semiconductor devices such as SiC (Silicon Carbide) based MOSFETs and diodes because they are very promissing and attractive as power switching devices for various kinds of near future power converters. The SiC based devices have the following remarkable features, which completely surpasses conventional Si (Silicon) based semiconductor devices:

(1) approximately ten times higher voltage ratings than the Si based semiconductor devices;

(2) 10^5 V/μs-class switching speed;

(3) as low on-resistance as 1/200 to 1/500 of the conventional MOSFETs; and

(4) over 300 °C junction temparature.

These very attractive features make it possible to improve power density as well as efficiency of the power converters dramatically. However, there still remain many problems to be solved from the veiwpoint of practical implimentation of such SiC based MOSFETs. One of the problems is to achieve an extremely high-speed operation without sacrificing the efficiency of the power converter. In general, parasitic capacitors of the MOSFET disturb high-speed switching because charging and discharging the parasitic capacitors make turn-on time and turn-off time longer. To make matters worse, as an on-resistance of the MOSFET becomes lower and the drain current becomes higher, the MOSFET tends to increase its parasitic capacitances because thickness and area of the device chip get thinner and larger. Similarly in the case of SiC power devices, the parasitic capacitances of the SiC based MOSFET are a great concern, which fades away the above excellent features.

It is necessary to reduce both of the turn-on time and the turn-off time to achieve high-speed switching of the MOSFET. Particuraly the turn-on time can be adjusted by controlling electrical charge to the parasitic input capacitance. Conventional approaches take some simple techniques to speed up the turn-on time, i.e., reducing the gate resistance of the MOSFET, and connecting a speed-up capacitor in parallel with the gate resistance. Recently another new gate drive circuit is proposed, which introduces inductive impulse superposition technique to drive the high-speed MOSFET. The superposed impulse gate current allows exteremely fast charge to the parasitic input capacitor of the MOSFET. On the other hand, it is difficult to reduce the turn-off time by the above mentioned techniques because a time constant to charge the parasitic output capacitance of the MOSFET dominantly determines the turn-off time. Effective approaches to reduce the turn-off time have not been established yet and are required for the future power converters to improve its power density sramatically.

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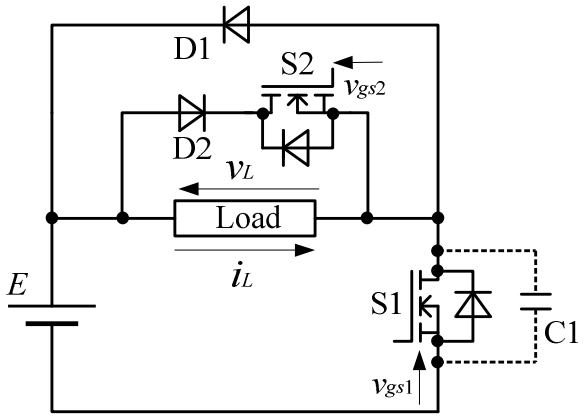

Fig. 1. Chopper with proposed auxiliary circuit.

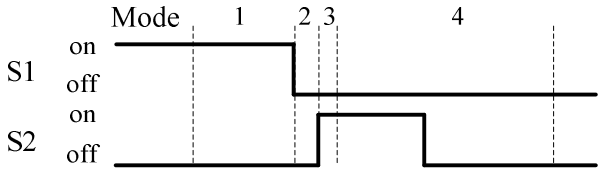

Fig. 2. Switching pattern of chopper with auxiliary circuit.

There are two manners to operate the power switching devices, i.e., one is a soft switching technique and the other is a hard switching technique. The former technique is basically emplyed to reduce switching losses as well as radiation and conduction noises. However, the technique can reduce the switching losses by lowering dv/dt and di/dt, while it seems to be rather difficult to achieve a high-frequency operation such as MHz-order switching because low dv/dt and di/dt increase the switching time.

This paper proposes a new approach to achieve a high-speed switching operation of the MOSFET with large parasitic output capacitors. The proposed approach is based on use of an auxiliary circuit shorting the load. The porpose of this auxiliary circuit is not the above mentioned soft switching but a hard swiching operation, so it makes a high-speed and high-efficiency switching possible by enlarging dv/dt. The proposed method is applied to a chopper and a half-bridge inverter as well. It has been confirmed through experimental tests that the chopper with the proposed auxiliary circuit can generate over 1-MHz output without deteriorated switching waveform and the half-bridge inverter with the extended auxiliary circuit can improve its total efficiency by 8 points in a low-load range compared with the conventional inverter.

II. Circuit Configration and Operation

A. Chopper with Auxiliary Circuit Shorting Load

Figure 1 shows a chopper with a proposed auxiliary circuit that consists of an additional auxiliary diode D2 and an auxiliary switch S2. This auxiliary circuit is directly connected in parallel with the load, which makes unidirectional current flow possible with shorting the load. The DC power supply voltage E is 100 V, the main power switching device S1 and the auxiliary switch S2 are FK-30SM-5, MITSUBISHI, and the auxiliary diode D2 is STTH60L06, ST Microelectronics. The load is an inductive load. C1 specifically shown in the figure is

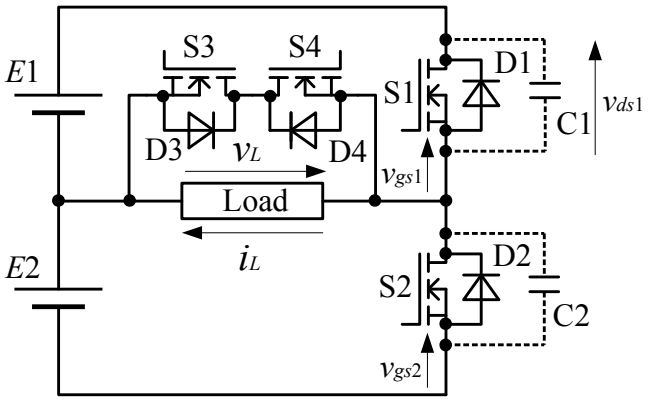

Fig. 3. Half-bridge inverter with proposed auxiliary circuit.

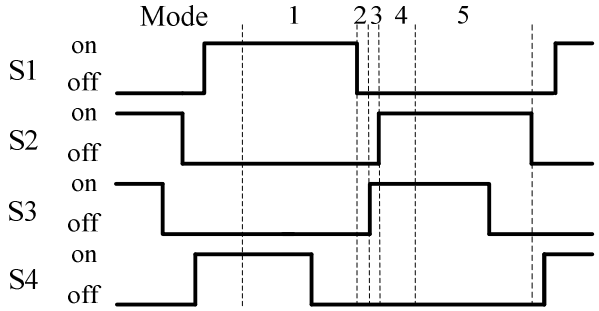

Fig. 4. Switching pattern of inverter with auxiliary circuit.

a parasitic output capacitor of the main device S1, of which capacitance is 580 pF. None of the parasitic capacitors of the auxiliary switch S2 are shown in Fig. 1 because they are negligibly small compared with those of the main device S1. The current rating of the auxiliary switch S2 is not needed to be high because the drain current of the auxiliary switch S2 does not flow continuously. Since the auxiliary switch S2 requires high-speed switching at turn-on, a device with a small parasitic input capacitor should be employed.

Figure 2 shows a switching pattern of the chopper with the proposed auxiliary circuit shorting load. In the figure, only a turning-off operation of the main device S1 is illustrated because the auxiliary circuit works at only the timing of the turn-off of the main device S1. The auxiliary switch S2 turns on right after the turn-off of S1. The current in Mode 1 flows in a path of E→Load→S1→E, and the main device S1 turns off at the end of the Mode 1. The auxiliary switch S2 must be turned on as soon as the gate signal to the main device S1 goes down. However, it takes certain time to turn on S2 and to turn off S1 completely. Mode 2 is a period that both of the switching devices are in such a transient state. In the Mode 2, the current still flows in the path of E→Load→S1→E, and charging the parasitic output capacitance of S1 gets started. In this short period of the Mode 2, the charging speed is not fast because the drain-source voltage rises according to a time constant determined by the load and the parasitic output capacitance C1. Therefore, the rising time of S1 depends on the load current, and the lower load current makes the turn-off time longer. In other words, it is difficult to achieve a fast switching of S1 in a low-load range.

In order to solve the above problem, the proposed method introduces the auxiliary circuit shorting load, which provides the parasitic output capacitance C1 with a fast chargeable current path. By turning on the auxiliary switch S2, the current path of E→D2→S2→C1→E is established to charge the parasitic output capacitance C1 very rapidly, and the turn-off time of S1 can effectively be improved. The charging current of C1 is independent of the load current, so the fast switching of S1 can be obtained even in the low-load range. After completing the turn-off process of S1, i.e., charging process of C1, the proposed circuit gets into Mode 4, and the load current circulates in the loop of Load→D1→Load like a conventional buck chopper.

B. Haif-Bridge Inverter with Auxiliary Circuit Shorting Load

Figure 3 shows a proposed half-bridge inverter with another configuration of an auxiliary circuit. Since the load current and the load voltage are bipolar in the case of the inverter, the auxiliary circuit must be a bidirectional and four-quadrant switch. This is the reason why two sets of MOSFETs with body diodes are connected in parallel with the load. The proposed configuration of the inverter looks identical to the neutral point shorted or the T type three-level inverter, but the purpose and the operation of the auxiliary circuit is far different from those of the conventional three-level inverter. In other words, the proposed inverter does not work to generate the three-level output voltage although the bidirectional switch is connected to the load.

The power supply voltage $E1$ and $E2$ are 100V, the main devices S1 and S2 are STY60NM60, ST Microelectronics, auxiliary switches S3 and S4 are FK30SM-5, MITSUBISHI, and the load is inductive of which power factor is 0.85. C1 and C2 represent parasitic output capacitors of the main devices S1 and S2. As described in the previous section, parasitic capacitors of the auxiliary switches S3 and S4 are omitted from Fig.3 because of their negligibly smaller values compared with those of the main devices. It is possible to employ low-current and half-voltage rated switching devices in the auxiliary circuit as the load current does not flow continuously through the auxiliary circuit. Instead transient pulse-shaped current flows through only in a turning-off moment of the main devices S1 and S2.

Figure 4 shows a switching pattern of the half-bridge inverter with the proposed auxiliary circuit shorting the load. One of the auxiliary switches S3 and S4 turns on just after one of the main devices S1 and S2 turns off. In Mode 1, it is assumed that the load is drawing the current in a path of $E1$→S1→Load→$E1$. The parasitic output capacitance C2 has been charged at the voltage of $E1$+$E2$ in this mode. By turning off S1, charging of the parasitic output capacitance C1 gets started in the path of $E1$→C1→Load→$E1$, whereas the other parasitic output capacitance C2 is discharged in the path of C2→Load→$E2$→C2 at the same time. In this short transient period, the charging time and the discharging time are governed by time constants between the load and each parasitic output capacitance of the main device. Therefore, this transient period becomes longer as the load current gets lower. In other words, it is more difficult to achieve fast switching operation as the load is reduced, especially in a low-load range. When the

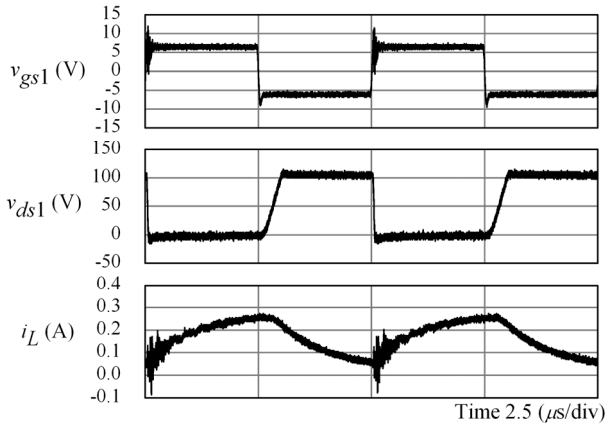

Fig. 5. Experimental waveforms of conventional chopper at 200-kHz output.

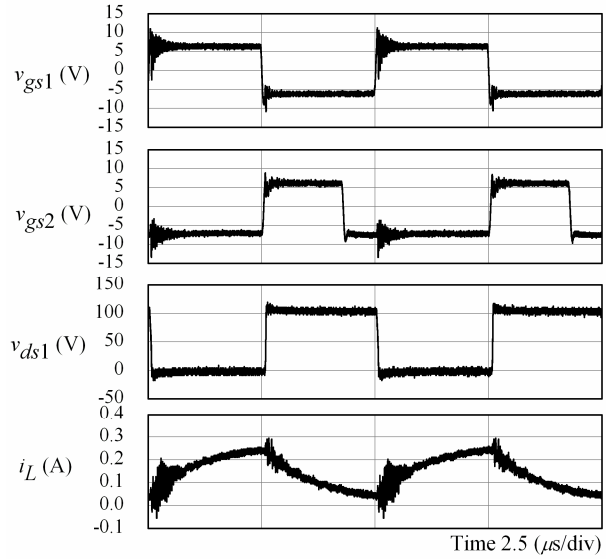

Fig. 6. Experimental waveforms of proposed chopper at 200-kHz output.

dead time period to prevent a short circuit across the DC bus is completed during this charging and discharging period of the parasitic output capacitances, the other main device S2 is turned on. Turning on S2 dissipates energy stored in the parasitic output capacitance C2, and a short circuit current flows through C1 and S2 in the path of $E1$→C1→S2→$E2$→$E1$. Therefore, one of the auxiliary switch S3 is turned on as soon as the main device S1 is turned off to make the fast switching possible. By turning on the auxiliary switch S3 in Mode 3, the parasitic output capacitance C1 is charged rapidly through the path of $E1$→C1→D4→S3→$E1$. The other parasitic output capacitance C2 is discharged quickly through the path of C2→D4→S3→$E2$→C2 at the same time. This operation mode allows to retrieve the energy stored in C2 to E2, which contributes to improve total efficiency of the whole inverter circuit. The current path in this period is independent of the load, so the fast switching can be achieved even in a low-load condition. In Mode 4, electrical charge remained in the parasitic output capacitance C2 is consumed by turning on S2 while the other parasitic output capacitance C1 is charged quickly owing to a short current of $E1$→C1→S2→$E2$→$E1$. The short current at this moment can be mitigated, compared the proposed circuit with the conventional one. After the

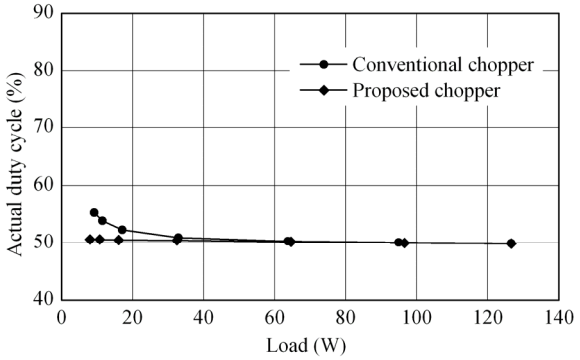

Fig. 7. Load to actual duty cycle characteristic.

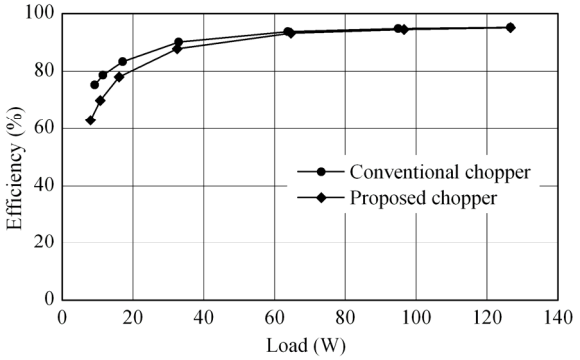

Fig. 8. Load to efficiency characteristic.

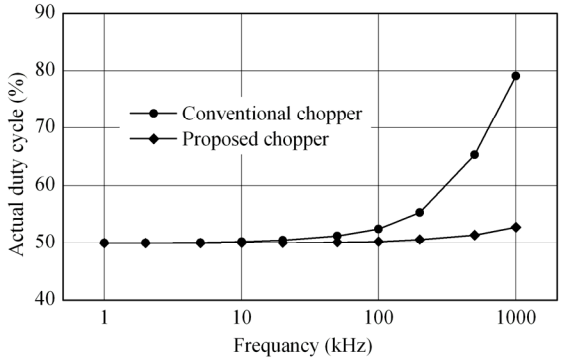

Fig. 9. Operation frequency to actual duty cycle characteristic.

circulating load current mode (Load→*E*2→D2→Load) in the Mode 4, Mode 5 gets started and lets the load current flow through the path of *E*2→Load→S2→*E*2. A similar operation is performed when the main device S2 is turned off and S1 is turned on.

III. Experimental Test Results

A. Chopper with Auxiliary Circuit Shorting Load

Some experimental tests have been conducted to examine feasibility of the proposed technique. Figures 5 and 6 show operation waveforms of the conventional chopper and the chopper with the proposed auxiliary circuit, respectively. In both prototype circuits, operation frequency is 200 kHz, the duty cycle is 50 %, and the load is 400 Ω and 0.4 mH. As can be seen in Fig. 5, the drain-source voltage v_{ds1} rises very slowly in the conventional chopper due to the parasitic output

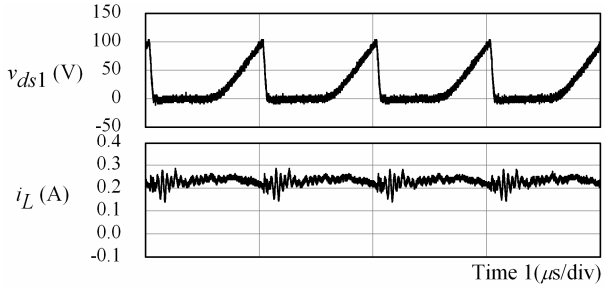

Fig. 10. 1-MHz output waveforms of conventional chopper.

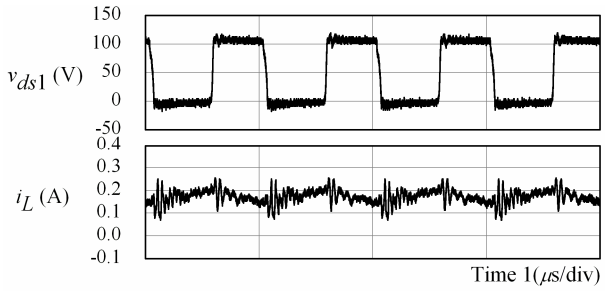

Fig. 11. 1-MHz output waveforms of proposed chopper.

capacitance of the main device. It takes a long time to charge fully the parasitic output capacitance, which results in the slow turning off of the main device. On the other hand, very rapid rising of v_{ds1} can be confirmed as shown in Fig. 6. This fast switching operation is achieved by turning on the auxiliary switch S2 just after the main device S1 is turned off. Even though the same gate signals at the duty cycle of 50 % are applied to the both choppers, actual duty cycles of the drain-source voltage waveforms are 55.3 % and 50.6 %, respectively. In addition, according to the turn off d*v*/dt of v_{ds1} in Figs. 5 and 6, very high rate of 8.0 kV/μs can be confirmed with the proposed circuit, which is approximately 26 times of d*v*/dt of the conventional circuit. Figure 7 indicates a load to actual on-duty cycle characteristic under the condition of a constant load power factor at 0.62. It can be seen that the proposed circuit is capable to operate around 50 % actual duty cycle even in a low-load range. Both of the conventional and proposed choppers can operate at 50 % actual duty cycle if they have a heavy load, i.e., a high load current, because the high load current allows quick charge of the parasitic output capacitance in the both cases. Figure 8 shows a load to total efficiency characteristic. As shown in the figure, the conventional circuit has better result than the proposed one in the low-load range less than 63 W. This efficiency degradation of the proposed circuit is caused by a switching loss and a conduction loss of the auxiliary circuit. However, the proposed technique makes it possible to operate the chopper at very high operation frequency. Figure 9 shows an actual duty cycles of v_{ds1} when the operation frequency is varied up to 1 MHz under the condition of a 400-Ω constant load. As shown in the figure, the proposed circuit is capable to operate at almost 50 % actual duty cycle over the range of 1 MHz, whereas the conventional circuit is limited to work under 100 kHz. The actual duty cycles of the both circuits are 79.1 % and 52.8 % at 1-MHz operation frequency, respectively. Figures 10 and 11 indicate the 1-MHz output waveforms of the conventional and the proposed choppers. As shown in Fig. 10, the MOSFET of the conventional circuit does not work as a switch at 1 MHz

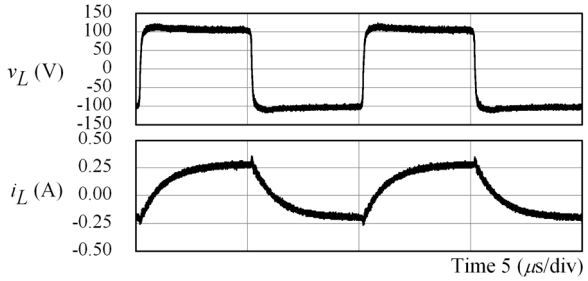

Fig. 12. Experimental waveforms of conventional inverter at 100-kHz output.

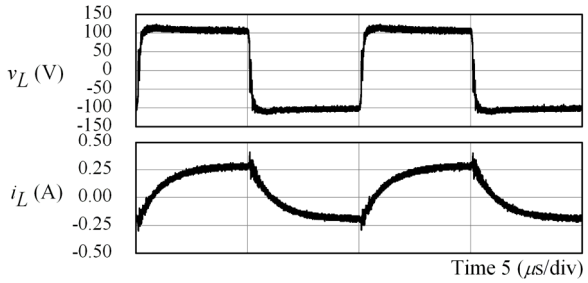

Fig. 13 Experimental waveforms of proposed inverter at 100-kHz output.

because its slow rising time is dominant in the switching period. As described above, the chopper with the proposed auxiliary circuit has slightly lower efficiency in the low-load range, but is capable to operate properly over the frequency range of MHz-class.

B. Haif-Bridge Inverter with Auxiliary Circuit Shorting Load

Two prototypes of a conventional inverter and an inverter with a proposed auxiliary circuit have been set up to confirm their operation characteristics. These inverters are operated at an operation frequency of 100 kHz, a duty cycle of 50 %, a dead time of 150 ns, and a load of 400 Ω plus 0.4 mH. Their operating waveforms are shown in Figs. 12 and 13. As can be seen in the figures, there is hardly big difference between the output voltages and the load currents of both inverters. Since the dead time to prevent a short circuit across the DC bus is only 150 ns, and the auxiliary circuit works only in the dead time period, which does not affect the operating waveforms detrimentally. Enlarged waveforms are depicted in Figs. 14 and 15 where the gate-source voltage v_{gs1}, the drain-source voltage v_{ds1} and the load voltage v_L are observed in detail. As can be seen in these figures, the rising time of the drain-source voltage waveform v_{ds1} of the proposed circuit is effectively improved, and it should be noted that the delay time between the falling edge of the gate signal v_{gs1} and the rising edge of the drain-source voltage v_{ds1} is remarkably reduced by the proposed technique. There is a dead to time to prevent a short circuit across the DC bus between turning-off operation of S1 and turning-on operation of S2. One of the auxiliary switch S3 is turned on within the dead time period. The parasitic output capacitance C1 is rapidly charged through the path of *E*1→C1→D4→S3→*E*1, and energy stored in the other parasitic output capacitance C2 is simultaneously retrieved to the power source *E*2 through the path of C2→D4→S3→*E*2→C2. This implies that energy consumption of the electrical charge stored in C2 can be diminished when the main device S2 is turned on, which leads to reduction of the turn-on loss of the main devices. In the case

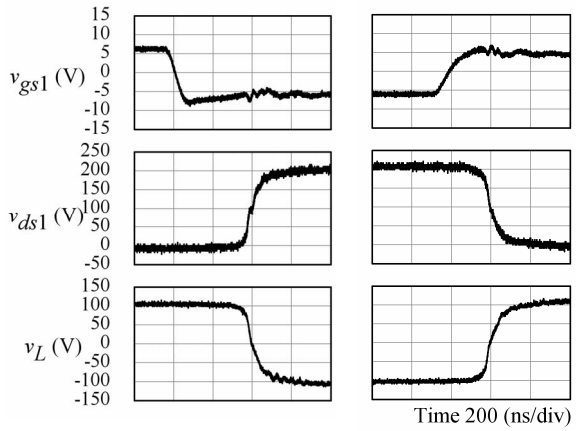

Fig. 14. Enlarged waveforms of conventional circuit.

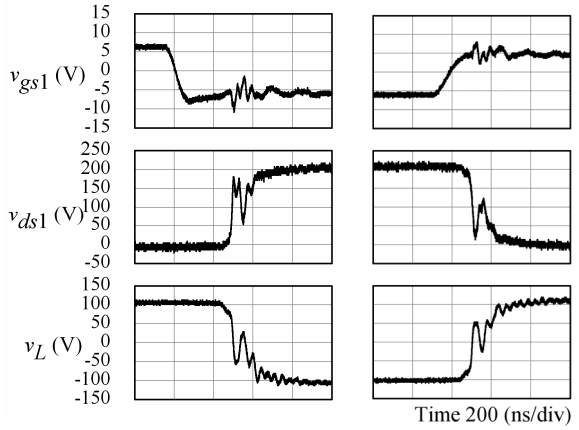

Fig. 15. Enlarged waveforms of proposed circuit.

of the conventional chopper, the time delay between the falling edge of the gate signal v_{gs1} and the rising edge of the drain-source voltage vds1 is 380 ns. However, the time delay of the proposed circuit can be reduced to 288 ns, and the total efficiency is improved from 53.9 % to 60.0 %. As described so far, not only speeding up the turn-off operation but also improving the efficiency can be realized by the proposed technique.

Figure 16 shows an efficiency characteristic of the conventional and the proposed inverters. It is found that the efficiency of the proposed circuit is higher than that of the conventional one in the low-load range under 28 W. The maximum difference between the two efficiency characteristics is 6.1 points at the lowest load condition of 14 W. This efficiency improvement is chiefly achieved by diminishing the turn-on loss of the main devices after the dead time period. In addition, a relationship between the dead time and the efficiency is indicated in Fig. 17, where the load is kept constant at 14 W. It can be seen that the longer dead time makes turn-on loss lower and the total efficiency higher because even the conventional circuit can charge or discharge the parasitic output capacitance of the main devices during the dead time. In general, however, it is desirable to set the dead time less than 5 % of the switching period, so the dead time shorter than 500 ns is required in the 100-kHz prototype inverter. When the 100-kHz inverter is operated in low-load condition, it is impossible to charge or discharge the parasitic

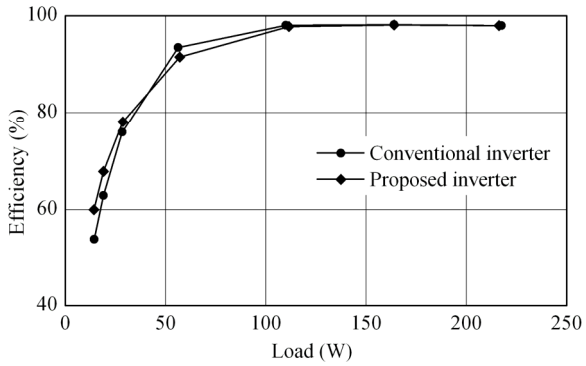

Fig. 16. Load to efficiency characteristic.

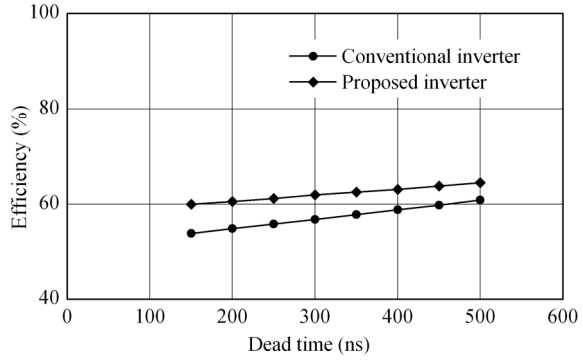

Fig. 17. Dead time to efficiency characteristic.

output capacitance quickly during the dead time. Therefore, the proposed auxiliary circuit is very effective to achieve high-speed switching as well as high-efficiency switching. As can be seen in Fig. 17, the efficiency of 60 % can be obtained at 150-ns dead time by the proposed technique, but the conventional circuit requires 450-ns dead time to achieve 60-% efficiency.

Since the conduction loss and the switching loss are dominant factors of power conversion losses and the conduction loss is almost same level between the conventional and the proposed circuit, the efficiency improvement of the proposed one owes reduction of the switching loss and retrieval of the energy stored in the parasitic output capacitance. The proposed technique is considered to be effective and efficient when the MHz-class high-frequency power converters are operated.

IV. Conclusion

This paper has described a high-speed switching operation of MOSFETs using an auxiliary circuit shorting the load. The proposed technique has been applied to a chopper and a half-bridge inverter, and their operation characteristics have been confirmed through several experimental tests.

As a result, the proposed circuit surpasses the conventional one particularly in a low-load range from various viewpoints. In the case of the chopper application, the proposed technique is capable to drive the main switching device over 1-MHz even in a low-load range, and the actual on-duty cycle of the main device is improved by 26.3 points from 79.1% to 52.8% when the commanded duty cycle of the gate signal is 50 %. Furthermore, it is confirmed that the turn-off dv/dt is enhanced from 0.3 kV/μs to 8.0 kV/μs; hence this means that the proposed technique can achieve 26 times high-speed switching of the main device in comparison with the conventional circuit.

On the other hand, the half-bridge inverter with the proposed auxiliary circuit is also possible to shorten the turn-off time from 380 ns to 288 ns even at a low output power of 14 W. It is confirmed that the total efficiency including the proposed auxiliary circuit can be improved by 6.1 points from 53.9 % to 60.0 % in such a low-load range. Moreover, the proposed technique can shorten the dead time from 450 ns to 150 ns if the same level of the total efficiency, e.g. 60 %, is required.

The proposed method is very effective to drive the MOSFETs with a large parasitic capacitance. Particularly, if multiple MOSFETs are connected in parallel to enhance the current capability, the method is suitable to such applications.

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