High-Speed Switching Method of MOSFET Using Voltage Boost Auxiliary Circuit Fed by Gate Drive Power Supply

-Applications to Chopper and Half-Bridge Inverter and Their Operation Characteristics -

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***Abstract*— This paper describes a high-speed switching method of MOSFETs applied to a chopper and a half bridge inverter. By using a voltage boost auxiliary circuit fed by the gate drive power supply, the turn-off time of the MOSFET can be effectively reduced, which enables a high-frequency drive and reduction of the switching loss. It was confirmed through experimental tests that the turn-off d*v*/dt of the MOSFET was drastically improved by 9 times with the proposed method, especially in the low-load range.**

Keywords—MOSFET, turn-off time, high-speed switching, auxiliary circuit, chopper, inverter

I. INTRODUCTION

In recent years great attention has been paid on next-generation semiconductor devices such as SiC (Silicon Carbide) based MOSFETs and diodes because they are very promising and attractive as power switching devices for varieties of near-future power converters. The SiC based devices have the following significant features, which completely surpasses conventional Si (Silicon) based semiconductor devices:

(1) approximately ten times higher voltage ratings than Si based devices;
(2) 10^5 V/μs-class switching speed;
(3) as low on-resistance as 1/200 to 1/500 of conventional MOSFETs; and
(4) over 300 °C junction temparature.

These are very attractive features to improve the power density as well as the efficiency of the power converters dramatically. However, there are still many problems to be solved from the viewpoint of practical implementation of such SiC based MOSFETs. One of the problems is an extremely high-speed operation without sacrificing the power converter efficiency. In general, the parasitic capacitors of the MOSFET disturb the high-speed switching operation because the turn-on and the turn-off times become longer due to the parasitic capacitors. To make matters worse, as the on-resistance becomes lower and the drain current becomes higher, the MOSFET tends to increase its parasitic capacitance. Similarly in the case of the SiC power devices, the parasitic capacitance is one of the great concerns, which may fade away the above excellent features.

It is necessary to reduce both of the turn-on time and the turn-off time to achieve high-speed switching of the MOSFET. Particuraly the turn-on time can be adjusted by controlling electrical charge to the parasitic input capacitance. Conventional approaches have been taking some simple techniques to speed up the turn-on time, e.g., reducing the gate resistance of the MOSFET, and connecting a speed-up capacitor in parallel with the gate resistor. Recently another new gate drive circuit is proposed, which introduces inductive impulse superposition technique to drive the high-speed MOSFET. The superposed impulse gate current allows exteremely fast charge to the parasitic input capacitor of the MOSFET. On the other hand, it is difficult to speed up the turn-off behaviour by tuning the gate drive circuit because the turn-off time is mainly determined by the charging time of the output capacitor across the source and the drain.

The percentage of the switching loss to the whole power loss becomes large in the high-frequency operation of the power converters. The parasitic output capacitor of the MOSFET used in the power converter such as the inverter cannot be discharged perfectly in the low-load range during the dead time period. As a result, the short circuit current flows through the switching device to charge up the output capacitor when the switching device turns on. The short circuit current is the major part of the switching loss it the light-load operations. In general, there are two manners to operate the power switching devices, i.e., one is a soft switching technique and the other is a hard switching technique. The former technique is basically employed to

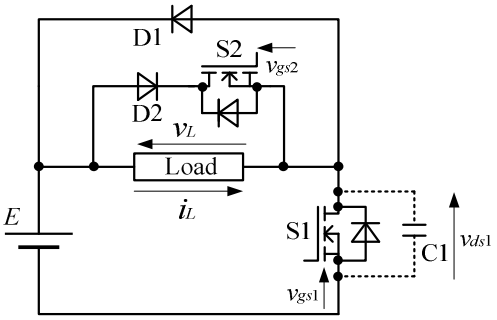

Fig. 1. Existing proposed buck chopper with auxiliary circuit.

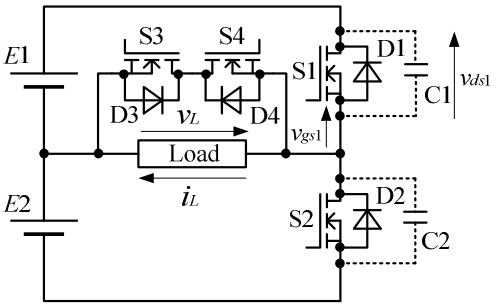

Fig. 2. Existing proposed half-bridge inverter with auxiliary circuit.

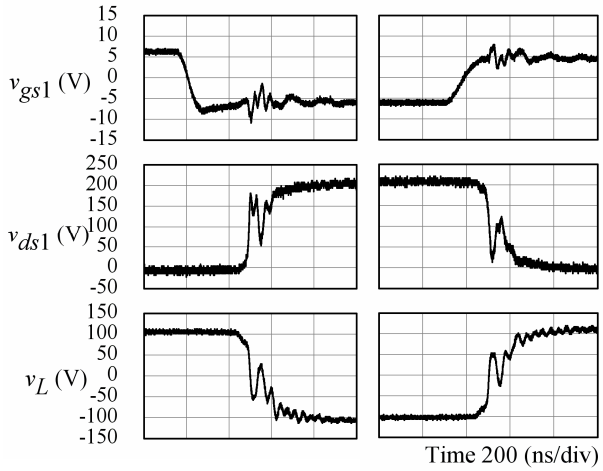

Fig. 3. Experimental waveforms of existing proposed inverter.

reduce the switching loss as well as the radiation and the conduction noises. However, the technique can reduce the switching loss by lowering d*v*/dt and d*i*/dt, so it is rather difficult to achieve a high-frequency operation of MHz-class because the lowered d*v*/dt and d*i*/dt increase the switching transient time.

The authors have proposed a new switching method of the MOSFET using a switching assist auxiliary circuit. The proposed method can reduce the turn-off time by connecting the auxiliary circuit in parallel with the load. However, the method has a drawback because it requires modification of the main circuit. Therefore, this paper proposes another new approach to achieve the high-speed switching operation of the MOSFET that has a large parasitic output capacitor. By using a voltage boost auxiliary circuit fed by the gate drive power supply, the high-frequency drive can be effectively carried out without any modification of the main circuit. The

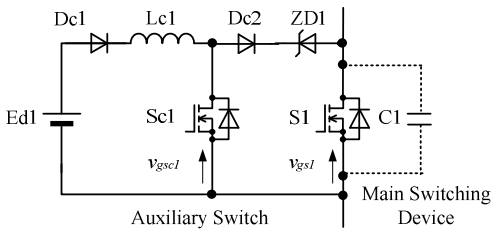

Fig. 4. Voltage boost auxiliary circuit fed by gate drive power supply.

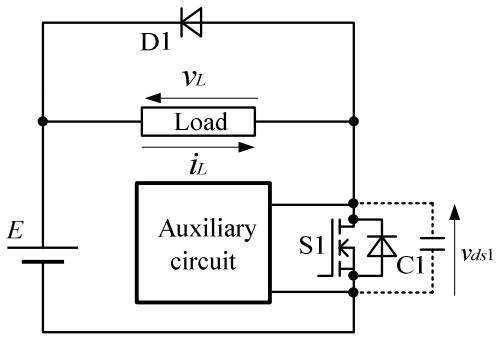

Fig. 5. Proposed buck chopper with auxiliary circuit.

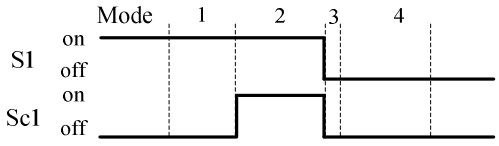

Fig. 6. Switching sequence of proposed chopper with auxiliary circuit.

purpose of this auxiliary circuit is not soft-switching but a hard-switching operation, and it makes not only the high-speed switching but also the high-efficiency operation possible by enhancing d*v*/dt. The proposed method is applied to a chopper and a half-bridge inverter as well in this paper.

II. Drawbacks of Existing Auxiliary Circuit

Figure 1 shows a chopper with the existing auxiliary circuit proposed by the authors, which consists of an additional auxiliary diode D2 and an auxiliary switch S2. Figure 2 shows another application of the existing auxiliary circuit to a half-bridge inverter, which consists of auxiliary switches S3 and S4. C1 and C2 are parasitic output capacitors of the main devices. The existing proposed method can reduce the turn-off time by shorting the load as soon as the main devices are turned off. However, they have some drawbacks as described below. First, modification of the main circuit is indispensable. Secondly, since the output capacitor of the main device is charged quickly by a high-d*i*/dt short circuit current, the resonance is caused, depending on the inductance of the current path and the output capacitor as shown in Fig. 3. The oscillation may cause malfunction when turning on the main devices. Thirdly, the on-timing control of the auxiliary devices is critically severe. If the auxiliary devices should be turned on before the main device is turned off, not only the main device but also the auxiliary devices would be destroyed by the short circuit current.

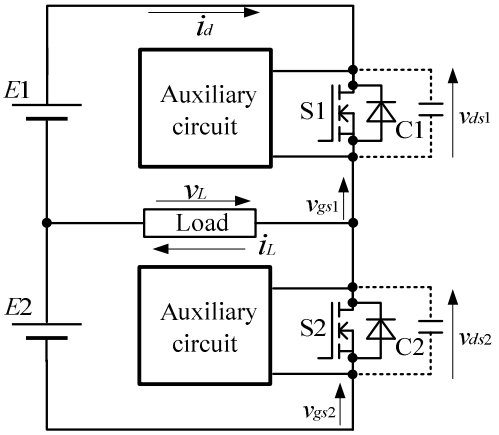

Fig. 7. Proposed half-bridge inverter with auxiliary circuit.

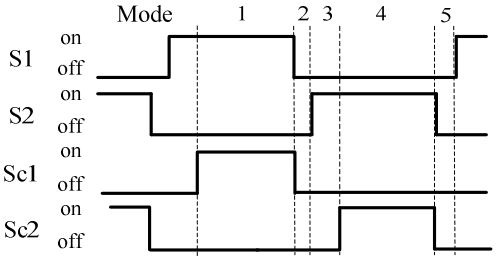

Fig. 8. Switching sequence of proposed inverter with auxiliary circuit.

III. Circuit Configurations and Operations

A. Chopper with Proposed Auxiliary Circuit

Figure 4 shows the voltage boost auxiliary circuit fed by the gate drive power supply. The proposed circuit is merely added to the gate drive circuit, so the modification of the main circuit is not required. The auxiliary circuit is composed of a gate drive power supply Ed1, auxiliary diodes Dc1 and Dc2, an inductor Lc1, a zener diode ZD1, and an auxiliary transistor Sc1. The gate drive power supply and the power source of the auxiliary transistor are on a common potential. Therefore, the auxiliary transistor and the main switching device can be driven by only a single gate drive power supply. A low-current rating device can be used as the auxiliary transistor to make the high-speed drive possible. The zener diode ZD1 is required to prevent the auxiliary circuit from circulating the current through S1 while S1 is turned on. Three zener diodes are actually connected in parallel because the individual current rating is low.

Figure 5 shows a buck chopper with the proposed auxiliary circuit. C1 is a parasitic output capacitor of the main switching device S1. The turn-off time of the conventional circuit is governed by a time constant determined by the load and the parasitic output capacitor of the main switching device. The turn-off time directly corresponds to a charging time of the parasitic output capacitor; thus, if the load resistance is high, the turn-off time becomes longer. Particularly it is difficult to speed up the switching time in the low-load range. In the proposed circuit, Sc1 is turned on prior to turning off S1 to store the energy in the inductor Lc1. Sc1 is turned off as soon as S1 is turned off to transfer the energy from Lc1 to C1.

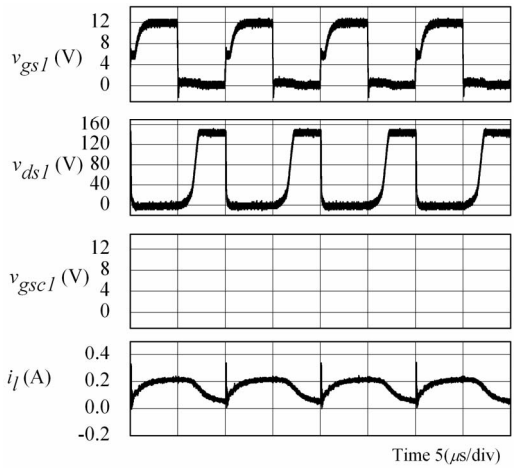

Fig. 9. Experimental waveforms of conventional buck chopper.

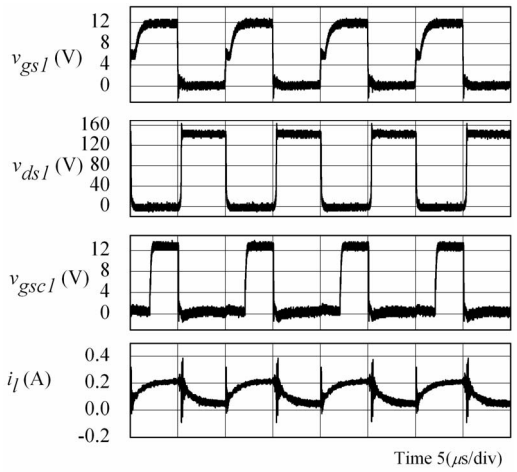

Fig. 10. Experimental waveforms of proposed buck chopper.

It makes the high-speed switching possible regardless of the load condition. Figure 6 shows the switching sequence of the proposed chopper. In the mode 1, the current flows through the path *E*→Load→S1→*E*. In the mode 2, the energy is charged in Lc1 through the path Ed1→Dc1→Lc1→Sc1→Ed1 by turning on Sc1. In the mode 3, the current flow commutates to the path Ed1→Dc1→Lc1→Dc2→ZD1→C1→Ed1 by turning off Sc1, so C1 is charged rapidly. The charging time of C1 is determined by the resonance frequency of Lc1 and C1, having nothing to do with the load current. The load current in the mode 4 circulates in the loop of Load→D1→Load.

B. Half-Bridge Inverter with Proposed Auxiliary Circuit

Figure 7 shows another application of the proposed auxiliary circuit to the half-bridge inverter. C1 and C2 are parasitic output capacitors of the main switching devices S1 and S2. During the dead time period, the charging time and the discharging time of C1 and C2 are governed by a time constant determined by the load and each of the parasitic output capacitors. If the dead time period is too short, turning on S1 dissipates the energy stored in C1, and the short circuit current flows through S1 by the path *E*1→S1→C2→*E*2→*E*1; hence the total efficiency decreases. In the proposed circuit,

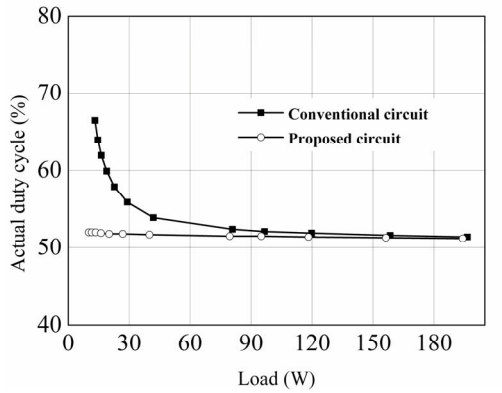

Fig. 11. Load-actual duty cycle characteristic.

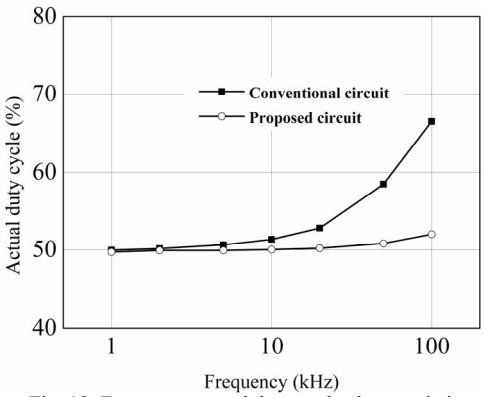

Fig. 12. Frequency-actual duty cycle characteristic.

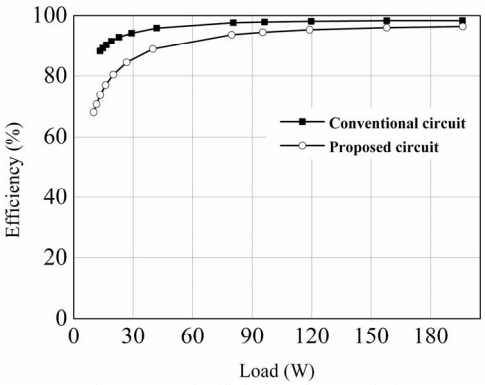

Fig. 13. Load-efficiency characteristic.

the auxiliary switch Sc1 is turned on prior to turning on S1 to store the energy in Lc1 like the proposed chopper does. Figure 8 shows the switching sequence of the proposed inverter. Sc1 is turned off as soon as S1 is turned on to transfer the energy from Lc1 to C1. By turning off Sc1, C1 is rapidly charged. Therefore, the short circuit current through the two of the main switching devices is effectively reduced, compared with the conventional circuit. This operation is performed in the same manner when S2 is turned off. The charging time is determined by the resonance frequency of Lc1 and C1, so d*v*/dt of the drain-source voltage becomes slightly lower than that of the conventional circuit. Therefore, the proposed circuit operates in a more stable fashion than the conventional circuit.

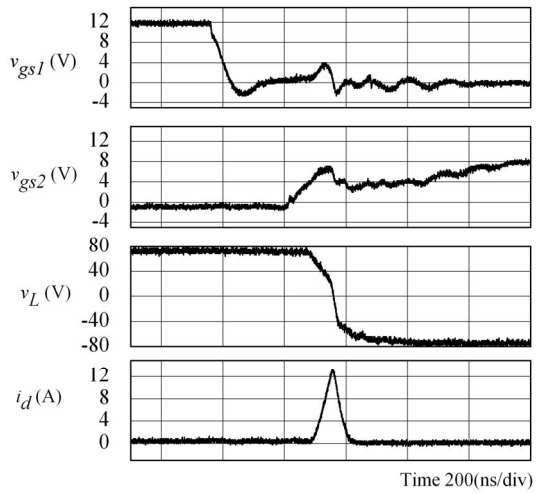

Fig. 14. Experimental waveforms of conventional inverter.

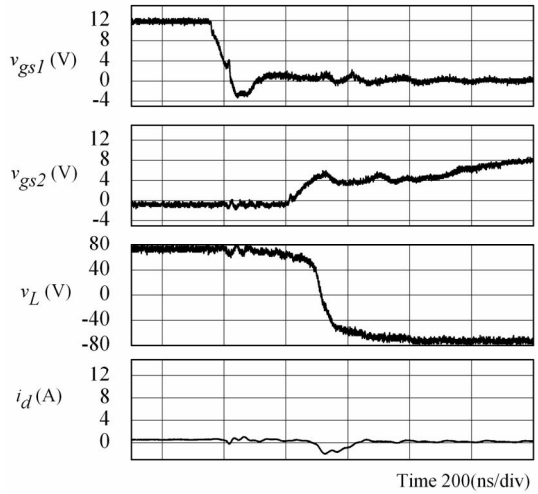

Fig. 15. Experimental waveforms of proposed inverter.

IV. Experimental Test Results

A. Operation Characteristics of Chopper

The experimental setup was built to confirm the operation characteristics of the proposed method. The experimental circuit has the same configuration as shown in Fig. 4, and is connected across the source and the drain of the main switching device. The main power supply voltage E is 140 V, S1 is STY60NM60 (ST microelectronics, Coss = 2000 pF), Ed1 is 12 V, Sc1 is STP12NM60 (ST microelectronics), Dc1 and Dc2 are D06S60 (ST microelectronics), the free-wheeling diode D1 is D12S60 (ST microelectronics), ZD1 is three parallel connected 1N5349BG (ON Semiconductor), Lc1 is 12 μH, and the load is inductive of which power factor is kept at 0.85.

Figures 9 and 10 show the output waveforms of the conventional and the proposed circuits under 13-W output condition. In order to achieve this operating condition, a 800-Ω and 0.8-mH RL load, a 100-kHz switching frequency, a 50 % duty cycle, and a 3-μs on-time of Sc1 are introduced to the system. In these figures, it can be found that the turn-off

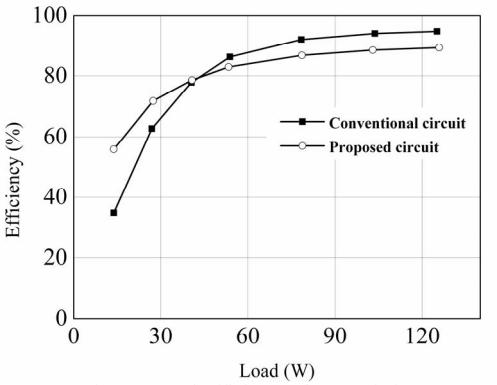

Fig. 16. Load-efficiency characteristic.

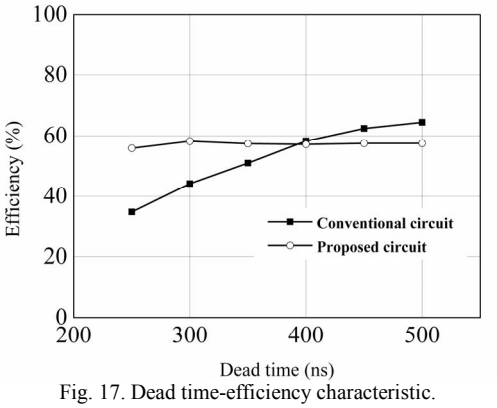

Fig. 17. Dead time-efficiency characteristic.

time of the proposed circuit is much shorter than that of the conventional circuit. Since C1 is charged quickly by using the proposed auxiliary circuit, the actual duty cycle of *vds*1 is improved from 66.4 % to 52.0 %. In addition, the turn-off d*v*/dts of *vds*1 are 0.16 kV/μs and 1.49 kV/μs, respectively, so the turn-off d*v*/dt of the proposed circuit is 9 times higher than that of the conventional circuit. Figure 11 shows a characteristic between the load power and the actual duty cycle of the main switching device. It can be seen in the figure that the proposed circuit always operates around 50 % even in the low-load range, while the conventional circuit can not achieve 50 % duty cycle operation in the range. This is because the output capacitor cannot be charged due to the low-load current in the low-load range. The actual duty cycle of the proposed circuit, however, is slightly deviated from 50 %, which corresponds to the charge time determined by the resonance frequency of Lc1 and C1. Figure 12 shows a frequency to the actual duty cycle characteristic. The actual duty cycle of the conventional circuit is far from 50 % in the high-frequency drive. On the other hand, the actual duty cycle of the proposed circuit can maintain around 50 % for any load range. Figure 13 shows a load to total efficiency characteristic including the auxiliary circuit power consumption. The efficiency of the proposed circuit is lower than that of the conventional circuit because the power loss in the auxiliary circuit is added to the total loss of the conventional circuit. It is confirmed that the efficiency of the proposed circuit is 15 pt lower than the conventional circuit.

It has been confirmed through the above experimental tests that the high-speed switching operation is possible by using the proposed auxiliary circuit technique.

B. Operation Characteristics of Half-Bridge Inverter

The experimental setup was built in the similar way as the chopper. The main power supply voltage *E*1 and *E*2 are 70 V, Dc1 is IDH12S60C (ST microelectronics), the inductors Lc1 and Lc2 are 4.5 μH, and other devices are same as the components used in the previously described chopper.

Figures 14 and 15 show the output waveforms of the conventional and the proposed circuits for 14-W output power. A 200-Ω and 0.2-mH RL load, a 100-kHz switching frequency, a 50 % duty cycle, a 250-ns dead time, and a 2-μs on-time of Sc1 and Sc2 are applied to the circuits. It is confirmed from Fig. 14 that the short circuit current i_d flows through the path *E*1→C1→S2→*E*2→*E*1. The short circuit is caused because one of the output capacitors C1 is not discharged during the dead time period. The gate voltage *vgs*1 oscillates just after S1 is turned off due to the high-d*i*/dt of the short circuit current flowing through the parasitic inductance along the current path. On the other hand, the short circuit current is remarkably reduced by the proposed circuit as shown in Fig.15. The output capacitor is charged quickly during the dead time period by using the proposed auxiliary circuit regardless of the load current. Therefore, the resonance of *vgs*1 is reduced owing to the low-d*i*/dt because the short circuit current does not flow. The turn-off times of S1 with and without the proposed auxiliary circuit are 450 ns and 390 ns, respectively. Figure 16 shows a load to total efficiency characteristic including the auxiliary circuit power consumption. It is confirmed from the figure that the total efficiency of the proposed circuit is higher than that of the conventional circuit in the low-load range. In the conventional circuit, the charging time and the discharging time of the output capacitor becomes longer in the low-load range, and short circuit current occurs across the DC bus. To make matters worse, the short circuit current flows though the main switching device when the device is turned on. However, the proposed circuit can charge and discharge the output capacitor quickly during the dead time period even in the low-load range, so the short circuit current can be dramatically reduced. The total efficiency is also improved by 9 points from 62.7 % to 71.7 % for 26-W output. Figure 17 shows a characteristic between the dead time and the total efficiency. The total efficiency of the conventional circuit is higher than that of the proposed circuit when the dead time is long because the output capacitor can be sufficiently charged and discharged even in the conventional circuit. In other words, the proposed circuit is significantly effective when the dead time should be shortened.

Generally, the dead-time period should be less than 5 % of the switching operation period. Therefore, it is required to determine the dead-time period less than 500-ns, when the operation frequency is 100-kHz, for example. In the case of the high-frequency drive such as 100-kHz, the output capacitors cannot be fully charged and discharged during the dead time period, so the proposed method is effective to make

the high-speed and high-frequency operation possible. Since the conduction loss and the switching loss are dominant factors among the power conversion losses and the conduction loss is almost same level between the conventional and the proposed circuits, the efficiency improvement of the proposed method mainly owes reduction of the switching loss. The proposed technique is considered to be effective and efficient for the MHz-class high-frequency power converters.

V. CONCLUSION

This paper has described a new high-speed switching operation technique of the MOSFET using the voltage boost auxiliary circuit fed by the gate drive power supply. The proposed circuit requires no modification of the main circuit. The technique has been applied to a chopper and a half-bridge inverter and their operation characteristics have been examined through several experimental tests.

As a result, the proposed circuit surpasses the conventional one particularly in the low-load range from various viewpoints. In the case of the chopper application, the actual duty cycle was improved by 14.4 pt from 66.4% to 52.0% when the duty cycle command of the gate signal was 50 %. Furthermore, it was confirmed that the turn-off dv/dt was enhanced from 0.16 kV/μs to 1.49 kV/μs; hence it meant that the proposed technique realized 9 times high-speed switching of the main switching device in comparison with the conventional circuit.

On the other hand, the half-bridge inverter with the proposed auxiliary circuit is capable to shorten the turn-off time from 450 ns to 390 ns even though as low-output-power as 14 W is demanded. It was confirmed that the total efficiency including the proposed auxiliary circuit power consumption was improved by 9 points from 62.7 % to 71.7 % for 26-W output condition.

The proposed method is very effective to drive the MOSFET with a large parasitic capacitance. Particularly, if multiple MOSFETs are connected in parallel to enhance the current rating, the method is more suitable to such high-power applications.

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