Switching Loss Reduction of MOSFET Using Switching Assist Circuit

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***Abstract*—This paper describes a new high-efficiency and high-speed switching method of a MOSFET using a switching assist circuit fed by the gate drive power supply. By applying the proposed circuit to a chopper and an inverter, a turn-off time of the MOSFET can be effectively reduced, which allows a higher-frequency operation and reduction of the turn-on loss. In the case of the application to the inverter, the total efficiency can be improved by 14.8 points in the low-load range owing to the reduction of the turn-on loss of the MOSFET.**

Keywords— MOSFET, high-speed switching, parametric design, turn-on ,turn-off, switching loss, auxiliary circuit, chopper, inverter

I. INTRODUCTION

In recent years, great attention has been paid to next-generation semiconductor devices such as SiC (Silicon Carbide) based MOSFETs and diodes because they are very promising and attractive as power switching devices for varieties of near-future power converters [1]-[5]. The SiC based devices have the following significant features, which completely surpasses conventional Si (Silicon) based semiconductor devices:

(1) approximately ten times higher voltage ratings than Si based devices;
(2) 10^5 V/μs-class switching speed;
(3) as low on-resistance as 1/200 to 1/500 of conventional MOSFETs; and
(4) over 300 °C junction temperature.

These are very attractive features to improve the power density as well as the efficiency of the power converters dramatically. However, there still remain many problems to be solved from the viewpoint of practical implementation of such SiC based MOSFETs. One of the problems is an extremely high-speed operation without sacrificing the power converter efficiency. In general, the parasitic capacitor of the MOSFET disturbs the high-speed switching operation because the turn-on and the turn-off times become longer due to the parasitic capacitor. To make matters worse, as the on-resistance becomes lower and the drain current becomes higher, the MOSFET tends to increase its parasitic capacitance. Similarly in the case of the SiC power devices, the parasitic capacitance is one of the great concerns, which may fade away the above excellent features.

It is necessary to reduce both of the turn-on time and the turn-off time to achieve high-speed switching of the MOSFET. Particularly the turn-on time can be adjusted by controlling electrical charge to the input parasitic capacitance. Conventional approaches have been taking some simple techniques to speed up the turn-on time, e.g., reducing the gate resistance of the MOSFET, and connecting a speed-up capacitor in parallel with the gate resistor. Recently another new gate drive circuit is proposed, which introduces an inductive impulse superposition technique to drive the high-speed MOSFET [6]-[9]. The superposed impulse gate current allows extremely fast charge to the parasitic input capacitor of the MOSFET, resulting in speed-up of the turn-on. On the other hand, it is difficult to speed up the turn-off behaviour by tuning the gate drive circuit because the turn-off time is mainly determined by the charging time of the output parasitic capacitor across the source and the drain. The authors have proposed a new switching method of the MOSFET using a switching assist circuit which makes a short circuit across the load [10]. The proposed method can reduce the turn-off time by connecting the auxiliary circuit in parallel with the load. However, the method has a drawback because it requires modification of the main circuit.

The percentage of the switching loss to the whole power loss becomes large in the high-frequency operation of the power converter. The output parasitic capacitor of the MOSFET used in the power converter such as the inverter cannot be discharged perfectly in the low-load range during the dead time period. Otherwise, the body diode of the MOSFET turns on during the dead time period. As a result, the short circuit current flows through the switching device to charge up the output parasitic capacitor when the corresponding counterpart switching device turns on. In addition, a large reverse recovery current is superimposed to the short circuit current when the body diode is turned off. The short circuit current causes the large turn-on loss which is the major part of the switching loss in the case of the light-load operation. The turn-on loss caused by the recovery current of the body diode can be reduced by using the

recovery assist circuit, but the charging current of the output parasitic capacitor cannot be suppressed [11].

In general, there are two manners to operate the power switching devices, i.e., one is a soft switching technique and the other is a hard switching technique. The former technique is basically employed to reduce the switching loss as well as the radiation and the conduction noises [12]-[17]. However, the technique can inherently reduce the switching loss by lowering dv/dt and di/dt, so it is rather difficult to achieve a high-frequency operation of MHz-class because the lowered dv/dt and di/dt increase the switching transient time.

Therefore, this paper proposes a new alternative approach to achieve the high-speed switching operation of the MOSFET with a large output parasitic capacitor. By using the proposed switching assist circuit fed by the gate drive power supply, the switching loss of the MOSFET can be effectively reduced without any modification of the main circuit [18]. The purpose of this auxiliary circuit is not a soft-switching but a hard-switching operation, and it makes not only the high-speed switching but also the high-efficiency operation possible by enhancing the dv/dt. The proposed method is applied to a chopper and a half-bridge inverter as well in this paper, and it has been confirmed that the switching assist circuit is effective to enchance the performance of the MOSFET.

II. MOSFET SWITCHING ASSIST CIRCUIT FED BY GATE DRIVE POWER SUPPLY

A. Configuration and Operation Principle of Proposed Auxiliary Circuit

Figure 1 shows the MOSFET switching assist circuit fed by the gate drive power supply, which is an application of the simple voltage boost converter. C1 is not a snubber circuit but an output parasitic capacitor of the main switching device S1. The gate drive power supply $Ed1$ and the power source of the auxiliary device Sc1 and S1 are connected on a common potential. Therefore, S1 and Sc1 can be driven by only a single gate drive power supply. The zener diode ZD1 is required to prevent the auxiliary circuit from circulating the current through S1 while S1 is turned on. Because the current rating of the zener diode is low, three devices are actually connected in parallel to enlarge the current rating.

In the conventional circuit of the power converter such as the buck chopper and the half-bridge inverter, if the main circuit current flows in the direction which charges C1, in other words, if the drain current of the MOSFET i_{d1} is positive, C1 is charged as soon as S1 is turned off. Therefore, the turn-off time is determined by i_{d1} and C1; thus, if i_{d1} is low enough, the turn-off time becomes longer. On the other hand, in the case of i_{d1} is negative, the body diode D1 turns on when the main switching device is turned off; hence C1 cannot be charged entirely. In the proposed circuit, Sc1 is turned on prior to turning off S1 to store the energy in the inductor Lc1. Sc1 is turned off as soon as S1 is turned off to transfer the energy from Lc1 to C1. It makes the high-speed switching possible regardless of the load power. Figure 2 shows the switching pattern of the auxiliary circuit. In the mode 1, the

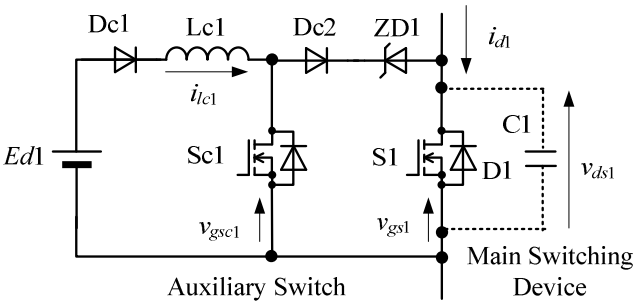


Fig. 1. Switching assist circuit fed by gate drive power supply.

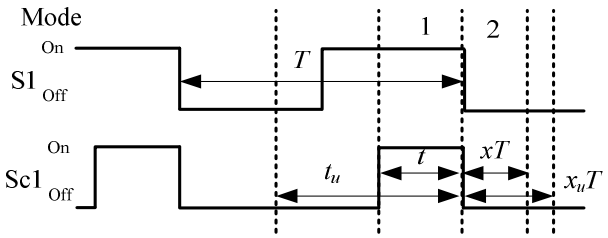


Fig. 2. Switching pattern of switching assist circuit.

energy is charged in Lc1 through the path $Ed1$→Dc1→Lc1→Sc1→$Ed1$ by turning on Sc1. In the mode 2, the current commutates to the path $Ed1$→Dc1→Lc1→Dc2 →ZD1→C1→$Ed1$ by turning off Sc1, so C1 is charged rapidly. When i_{d1} is positive, the energy of Lc1 can be transferred to the main circuit without consideration of the value of i_{d1}. However, if i_{d1} is negative, the current of Lc1 keeps flowing as a constant value which is determined by i_{d1} even if Sc1 is turned off. Therefore, the limited energy of the difference between i_{lc1} and i_{d1} is transferred. The charging time of C1 is basically determined by the resonance frequency of Lc1 and C1.

B. Parameter Design of Switching Assist Circuit

The parameters of the auxiliary circuit are designed, assuming that i_{d1} is zero. To achieve the high-speed switching by using the proposed circuit, the energy balance condition must be satisfied as expressed by

$$\frac{1}{2}C1{v_{ds1}}^2 = \frac{1}{2}Lc1{i_{lc1}}^2, \tag{1}$$

where v_{ds1} is the voltage applied across S1 and i_{lc1} is the peak current flowing through Lc1. i_{lc1} is determined by $Ed1$, Lc1, and t, where t is on-time duration of Sc1. Consequently, i_{lc1} is given as

$$i_{lc1} = \frac{Ed1}{Lc1}t\,. \tag{2}$$

By substituting (2) into (1), (1) can be rewritten as the following expression:

$$C1{v_{ds1}}^2 = \frac{{Ed1}^2}{Lc1}t^2\,. \tag{3}$$

Therefore, there still remain the undetermined parameters Lc1 and t in the auxiliary circuit, where other parameters v_{ds1}, $Ed1$, and C1 are already given. Hence, if either parameter of

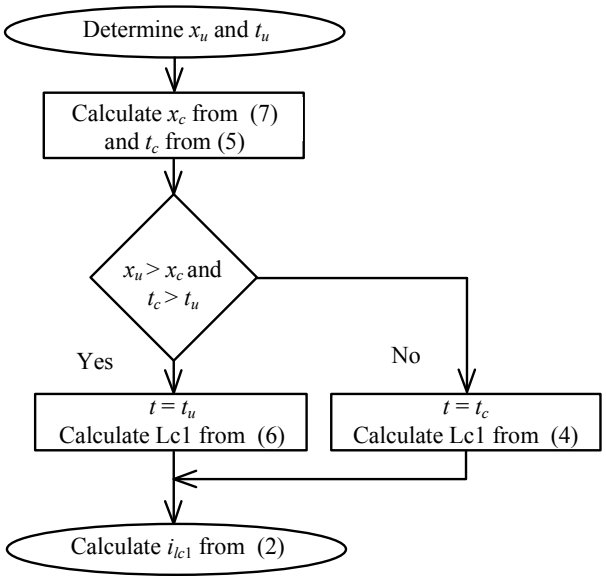


Fig. 3. Flow chart to determine parameters of switching assist circuit.

Lc1 or t is determined, the other parameter can be resultantly derived. The first method to determine the parameters is a way to design t after determination of Lc1. The charging time of C1 is determined by quarter of the resonance period governed by Lc1 and C1. Therefore, Lc1 can be simply expressed by

$$Lc1 = \frac{4x^2T^2}{\pi^2 C1}, \tag{4}$$

where T is the switching operation period of S1 and x is the charging time in percentage with respect to the operation period T. As a result, t can be calculated as follows:

$$t = \frac{v_{ds1}}{Ed1}\frac{2xT}{\pi}. \tag{5}$$

t must be within T, so it is difficult to make switching Sc1 possible if t is too long. Due to this restriction, when t reaches a certain prefixed time, this method is no longer applicable. Then any value x is defined as x_u (upper limit), and calculated t is defined as t_c (calculated value). The other method to design the auxiliary circuit parameters is a way to derive Lc1 under the condition of the given value of t. When on-time of Sc1 is t, Lc1 can be derived as

$$Lc1 = \left(\frac{Ed1}{v_{ds1}}\right)^2 \frac{t^2}{C1}. \tag{6}$$

In consequence, x is obtained as

$$x = \frac{\pi}{2T}\frac{Ed1}{v_{ds1}}t. \tag{7}$$

When x is too large, the auxiliary circuit is not effective to make the high-speed switching possible. Accordingly, if x reaches a constant predetermined percentage, this condition is no longer used. Then any value t is defined as t_u (upper limit),

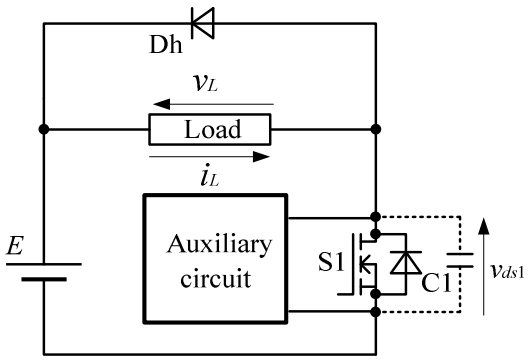


Fig. 4. Proposed buck chopper with auxiliary circuit.

and calculated x is defined as x_c (calculated value). The parameters of the auxiliary circuit are determined under the conditions that both calculated values x_c and t_c does not exceed the upper limits x_u and t_u, respectively. Figure 3 shows a flow chart to design the auxiliary circuit parameters. At the beginning of the flowchart, x_u and t_u are determined. x_c and t_c are calculated from (5) and (7). If $x_u > x_c$ and $t_c > t_u$, Lc1 is derived from (6) as $t = t_u$. On the other hand, if $x_c > x_u$ and $t_u > t_c$, Lc1 is determined from (4) as $t = t_c$. i_{lc1} is computed from (2) to select the appropriate switching device of the auxiliary circuit in terms of the current rating.

III. Applications of Proposed Auxiliary Circuit and Their Operation Characteristics

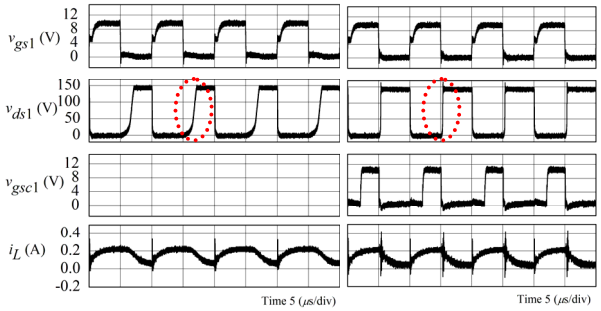
A. Buck Chopper with Proposed Auxiliary Circuit

This section describes that the output parasitic capacitor of the MOSFET can be quickly charged by applying the auxiliary circuit to a buck chopper. Figure 4 shows the buck chopper with the proposed auxiliary circuit. The turn-off time t_{off} of the conventional circuit is determined by i_{d1} and C1. Accordingly, t_{off} is given as

$$t_{off} = \frac{EC1}{i_L}. \tag{8}$$

Thus, if the load resistance is high, t_{off} becomes longer. Particularly it is difficult to speed up the switching time in the low-load range. In the proposed circuit, Sc1 is turned on prior to turning off S1 to store the energy in the inductor Lc1. Sc1 is turned off as soon as S1 is turned off to transfer the energy from Lc1 to C1. The proposed auxiliary circuit makes the high-speed switching possible regardless of the load condition. In this application, it is not necessary to care the relationship between i_L and the current charging C1 because i_{d1} is always positive.

The parameters of the auxiliary circuit are designed as follows: the main power supply voltage E is 140 V; S1 is STY60NM60 (C_{oss} = 2000 pF); $Ed1$ is 12 V; and the switching frequency is 100 kHz. When x_u is 2.5 % and t_u is 4 μs, t_c= 1.8 μs and x_c = 5.3 % are calculated from (5) and (7), respectively. As a result, t is t_c and Lc1 is derived to be 13 μH from (4) because $x_c > x_u$ and $t_u > t_c$. This derivation of the parameters is conducted in the ideal state, but there is a power consuming factor such as a forward voltage drop of the auxiliary diodes.



(a) Conventional circuit. (b) Proposed circuit.

Fig. 5. Experimental waveforms of buck chopper.

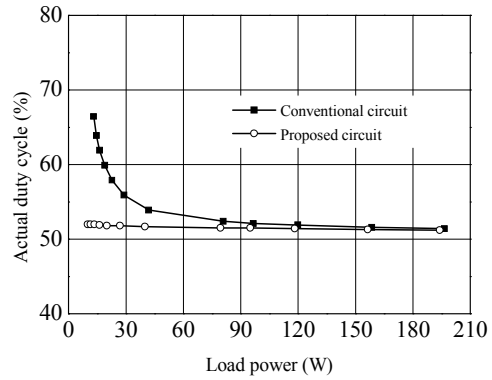


Fig. 6. Load power-actual on-duty cycle characteristic.

Therefore, t must be modified from 1.8 μs to 3 μs to satisfy (1), for example. i_{lc1} is calculated to be 2.8 A from (2) in this case. For this reason, STP12NM60 as Sc1, D06S60 as Dc1 and Dc2, and 1N5349BG as ZD1 are employed in the test circuit.

Figure 5 shows the output waveforms of the conventional and the proposed circuits for 13-W output power. In order to conduct the experiments in this operating condition, a 800-Ω and 0.8-mH RL load, a 100-kHz switching frequency, and a 50 % duty cycle are adopted to the test circuit. It is confirmed from the figures that t_{off} of the proposed circuit is much shorter than that of the conventional circuit. Since C1 is quickly charged by using the auxiliary circuit, the turn-off dv/dts of v_{ds1} are 0.16 kV/μs and 1.49 kV/μs, respectively, so the turn-off dv/dt of the proposed circuit is approximately 9 times higher than that of the conventional circuit. Figure 6 shows a characteristic between the load power and the actual duty cycle. It can be seen in the figure that the proposed circuit operates around 50 % regardless of the load power even in the low-load range, while the conventional circuit can no longer operate at 50 % duty cycle as the load power is reduced. This is because C1 cannot be charged due to the low-load current in the low-load range. It has been confirmed through the above experimental tests that the high-speed switching operation is possible by using the proposed technique.

B. 50 % Duty Cycle Rectangular Waveform Operation of Half-Bridge Inverter with Proposed Auxiliary Circuit

This section explains the turn-on loss reduction by means of reducing the short circuit current when the auxiliary circuit is applied to 50 % duty cycle rectangular waveform operation

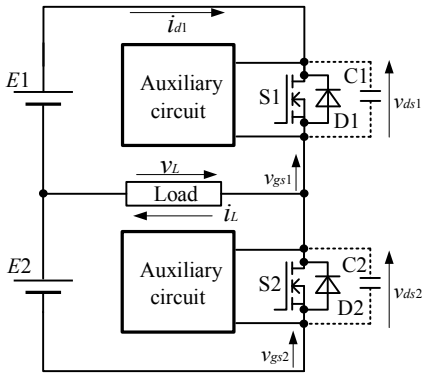


Fig. 7. Proposed inverter with auxiliary circuit.

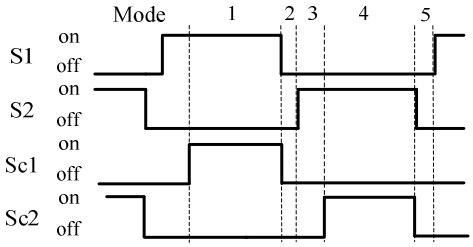
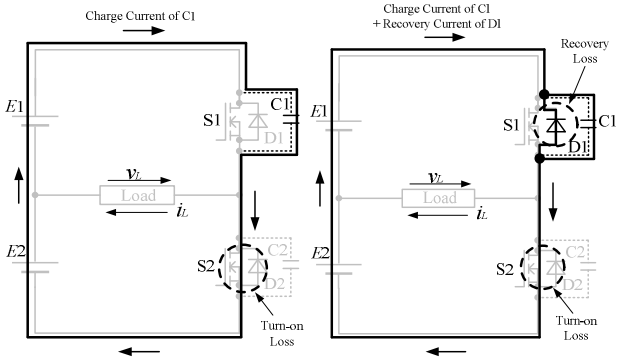


Fig. 8. Switching sequence of proposed inverter with auxiliary circuit.



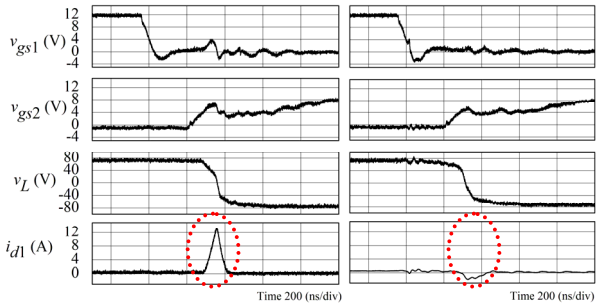
(a) Polarity of i_{d1} is positive (b) Polarity of i_{d1} is negative

Fig. 9. Short-circuit current path of conventional circuit.

of the half-bridge inverter. Figure 7 shows another application of the proposed auxiliary circuit to the half-bridge inverter, and Figure 8 shows the switching sequence of the proposed inverter. During the dead time period t_{dead} to avoid a short circuit across the DC bus, the charging time and the discharging time of C1 and C2 are determined by i_L and the total capacitance of C1 and C2. i_L required to charge the output parasitic capacitor perfectly during t_{dead} is obtained as (9)

$$i_L = \frac{(E1+E2)(C1+C2)}{t_{dead}}. \tag{9}$$

If t_{dead} is considerably short, the energy stored in C2 is dissipated by turning on S2, and the short circuit current flows through S2 in the path $E1 \rightarrow C1 \rightarrow S2 \rightarrow E2 \rightarrow E1$ as shown in Fig. 9(a); hence the total efficiency is detrimentally affected due to increase of the turn-on loss of S2. The on-resistance of main devices are high in the right moment of turning on the main devices, so the short circuit current becomes a key factor of the large turn-on loss. In the proposed circuit, however, C1



(a) Conventional circuit. (b) Proposed circuit.

Fig. 10. Experimental waveforms of 50 % duty cycle operation of inverter at 14-W output.

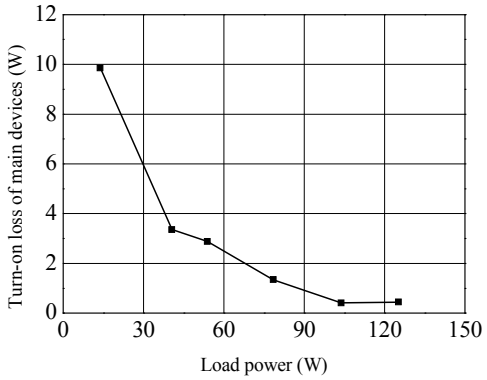


Fig. 11. Load power-turn-on loss of conventional circuit characteristic.

and C2 are quickly charged by using the auxiliary circuit just like the proposed chopper does. Therefore, the short circuit current through the two of the main devices can be effectively reduced, compared with the conventional circuit. It is not necessary to consider the load current polarity because i_{d1} always flows in the direction of charging the output parasitic capacitor in the moment of turning off the main devices.

The parameters of the auxiliary circuit are designed as follows: the main power supply voltage $E1$ and $E2$ are 70 V; S1 and S2 are STY60NM60 (C_{oss} = 2000 pF); $Ed1$ is 12 V; the switching frequency is 100 kHz; and t_{dead} is 250 ns. When x_u and t_u are determined to be 2.1 % and 4 μs, (5) and (7) give the values t_c and x_c of 5.4 % and 1.6 μs, respectively. t is t_c and Lc1 is calculated from (4) to be 4.5 μH because $x_c > x_u$ and $t_u > t_c$. This derivation of the parameters are conducted in the ideal state similarly to the buck chopper case. Therefore, t must be adjusted from 1.6 μs to 2 μs. i_{lc1} is reckoned to be 5.3 A from (2). Thus, Sc1 is STP12NM60, Dc1 is IDH12S60C, Dc2 is D06S60, and ZD1 are 1N5349BG.

Figure 10 shows the output waveforms of the conventional and the proposed circuits for 14-W output power. A 200-Ω and 0.2-mH RL load, a 100-kHz switching frequency, and a 50 % duty cycle are applied to the circuits. It is confirmed in Fig. 10(a) that the short circuit current flows because the output parasitic capacitor cannot be discharged during t_{dead}. Figure 11 shows the turn-on loss of the conventional circuit. It can be seen in the figure that the large turn-on loss is caused by this short circuit current in the low-load range. On the other hand, the short circuit current can be remarkably reduced by the proposed circuit as shown in Fig. 10(b). C1 and C2 are charged quickly during t_{dead} by using the proposed auxiliary

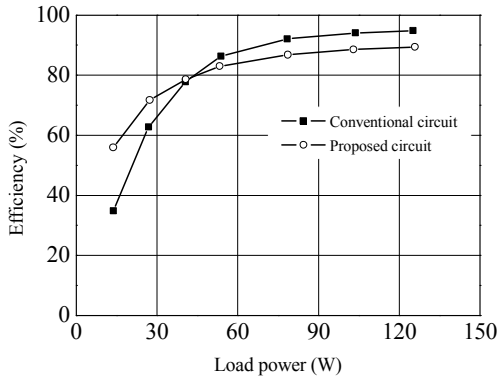


Fig. 12. Load power-efficiency characteristic

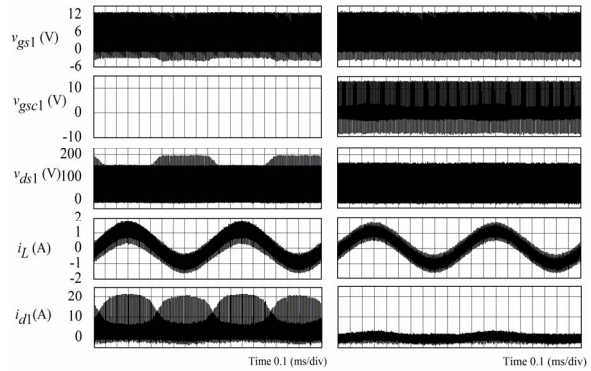
TABLE I. OPERATION MODES OF AUXILIARY CIRCUIT

Polarity of i_L	Threshold current of Sc1	Threshold current of Sc2
Positive	$I_{th1} = \frac{(E1+E2)(C1+C2)}{t_{dead}}$	I_{th2}
Negative	$I_{th2} = \frac{Ed1}{Lc1}t$	I_{th1}

circuit regardless of i_L. In addition, the turn-off times of S1 with and without the proposed auxiliary circuit are 450 ns and 390 ns, respectively. Figure 12 shows a load power to total efficiency characteristic including the power consumption of the auxiliary circuit. It is confirmed from the figure that the total efficiency of the proposed circuit is higher than that of the conventional circuit in the low-load range. The proposed circuit can charge and discharge the output parasitic capacitor quickly even in the low-load range, so the turn-on loss of the main devices caused by the short circuit current is dramatically reduced. As a result, the total efficiency can be improved from 62.7 % to 71.7 % for 26-W output power. By disabling the auxiliary circuit in the heavy-load range, it is possible to operate the inverter at higher efficiency without power dissipation of the auxiliary circuit. Because the high-efficiency range can be expanded by the auxiliary circuit, the proposed technique is effective for the applications that need a very wide load range.

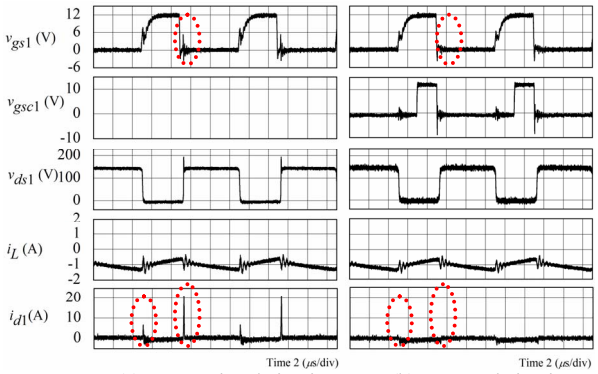
C. PWM Half-Bridge Inverter with Proposed Auxiliary Circuit

This section describes the reduction of the large turn-on loss caused by the charging current of the output parasitic capacitors and the recovery current of the body diodes, and explicates the control scheme of the auxiliary circuit in the application to the PWM half-bridge inverter. When one of the main switching devices turns off, the direction of the i_{d1} can be positive or negative because the carrier frequency is much higher than the load current fundamental frequency. If the polarity of i_{d1} is positive and the instantaneous amplitude of i_{d1} is high, it is not necessary to operate the auxiliary circuit as indicated by (9). The load current value which charges the output parasitic capacitor perfectly during t_{dead} is defined as I_{th1}, and the operation of the auxiliary circuit is disabled when i_{d1} is over I_{th1}. On the other hand, under the condition that the polarity of i_{d1} is negative, C1 is not charged at all even though the S1 turns off. Thus, the charging current of C1 flows to the



(a) Conventional circuit. (b) Proposed circuit.

Fig. 13. Experimental waveforms of PWM inverter at MI = 0.2.



(a) Conventional circuit. (b) Proposed circuit.

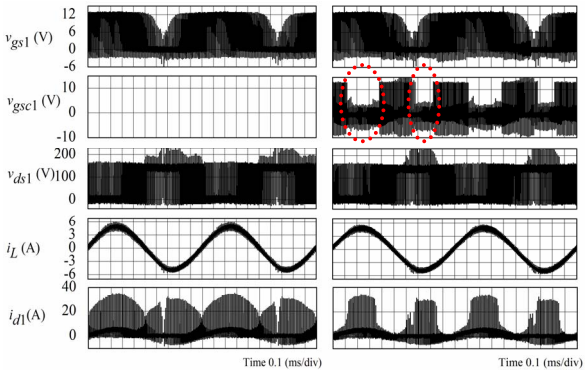
Fig. 14. Expanded views of experimental waveforms of PWM inverter at MI = 0.2.

path $E1 \rightarrow C1 \rightarrow S2 \rightarrow E2 \rightarrow E1$, and the recovery current of D1 commutates to the path $E1 \rightarrow D1 \rightarrow S2 \rightarrow E2 \rightarrow E1$ through S2 in the moment of turning on S2 as shown in Fig. 9(b). This short circuit current causes the large turn-on loss, so the efficiency is detrimentally deteriorated. In the proposed circuit, however, C1 is rapidly charged and D1 is turned off at the same time by using the auxiliary circuit. The recovery current of D1 flows to the path $C1 \rightarrow D1 \rightarrow C1$, so the turn-on loss of S2 is not caused since the DC bus is not short-circuited. However, the energy of Lc1 is not transferred perfectly to C1 because i_{lc1} still flows as the constant value which is determined by i_{d1} after Sc1 is turned off. The energy which can be transferred to the output parasitic capacitor P_t is determined by the energy difference between i_{lc1} and i_{d1}. P_t is simply expressed by

$$P_t = \frac{1}{2} Lc1 (i_{lc1}{}^2 - i_{d1}{}^2). \quad (10)$$

The load current value is defined as I_{th2} when P_t is zero. The auxiliary circuit is no longer operated if i_{d1} is over I_{th2}. As described above, it is necessary to divide the operation modes by the value and the polarity of i_{d1} which is determined by i_L and the mode classification of the auxiliary circuit as shown in TABLE I.

The all parameters of the experimental setup other than the load resistance are the same as those described in the previous section, and the fundamental operation frequency is identical to that of the 50 % duty cycle operation of the half-bridge inverter. I_{th1} = 2.2 A and I_{th2} = 5.3 A are calculated from TABLE I. These threshold currents are calculated in the



(a) Conventional circuit. (b) Proposed circuit.

Fig. 15. Experimental waveforms of PWM inverter at MI = 0.9.

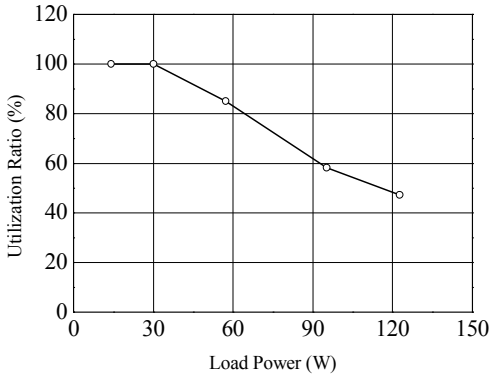


Fig. 16. Load power-utilization ratio characteristic.

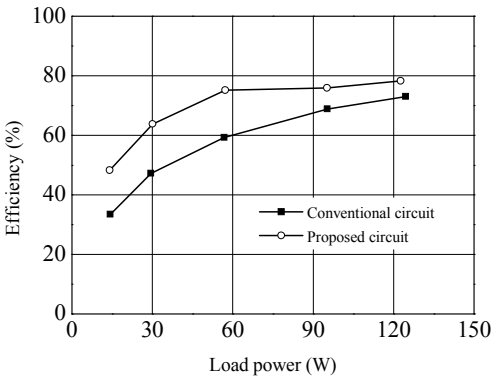


Fig. 17. Load power-efficiency characteristic.

ideal state, but C1 and C2 have voltage dependence and there are power consuming factors such as a forward voltage drop of the auxiliary diode. Hence, I_{th1} and I_{th2} must be slightly modified from 2.2 A to 3.0 A and 5.3 A to 4.0 A, respectively.

Figures 13 and 14 show the output waveforms of the conventional and the proposed circuits for 14-W output power. An 8-Ω and 1-mH RL load, a 100-kHz switching frequency, a 1-kHz operating frequency, and a 0.2 modulation index (MI) are applied to the circuits. It is confirmed in Figs. 13(a) and 14(a) that the DC bus is short-circuited by the charging current of the output parasitic capacitors and the recovery current of the body diodes. In addition, the gate voltage v_{gs1} oscillates just after S1 is turned off due to the high di/dt of the short circuit current flowing through the parasitic inductance along the current path. However, it is clear that this short circuit

current do not flow across the DC bus by using the auxiliary circuit as demonstrated in Figs. 13(b) and 14(b). Furthermore the oscillation of v_{gs1} is effectively suppressed by the low dv/dt determined by the resonance frequency of Lc1 and the output parasitic capacitors. The reduction of the short circuit current and the noise mean that the output parasitic capacitor is charged and the body diode turns off before the other counterpart main device turns on. The auxiliary circuit is always operated because the i_L is lower than the threshold current owing to the low MI. Figure 15 shows the output waveforms of the conventional and the proposed circuits in the heavy-load range. It is confirmed from this figure, the mode switching of the auxiliary circuit is properly performed when the load current is over the threshold current. In addition, it is observed that the short circuit current is effectively reduced as well as the low-load case. Figure 16 shows a load power to utilization ratio characteristic. In the heavy-load range, the utilization ratio of the auxiliary circuit decreases because the amplitude of i_L is high. Figure 17 shows a load to total efficiency characteristic including the power consumption of the auxiliary circuit. The efficiency of the proposed circuit is higher than that of the conventional circuit because the turn-on loss of the main devices is improved; thus, the efficiency of the proposed circuit is improved by 14.8 pt, compared with the conventional circuit at 14-W output power.

In general, the dead-time period should be less than 5 % of the switching operation period. In the case of the high-frequency drive such as 100-kHz, the output parasitic capacitors cannot be fully charged and discharged during the dead time period, so the proposed method is very effective to make the high-speed and high-frequency operation possible. Since the conduction loss and the switching loss are dominant factors among the power conversion losses, and the conduction loss is at almost the same level between the conventional and the proposed circuits, the efficiency improvement of the proposed method mainly owes reduction of the switching loss. The proposed technique is considered to be effective and efficient for the MHz-class power converters. The size of the power converters becomes compact in the case of the high-frequency operation because the filter inductor and the filter capacitor can be miniaturized.

IV. Conclusion

This paper has described a high-efficiency and high-speed switching operation technique of the MOSFETs using the switching assist circuit fed by the gate drive power supply. The designed auxiliary circuit has been applied to a chopper and a half-bridge inverter, and their operation characteristics have been confirmed through several experimental tests.

In the case of the chopper, it was confirmed that the turn-off dv/dt of the proposed circuit was 9 times higher than that of the conventional circuit.

On the other hand, in the case of the half-bridge inverter, the total efficiency was improved from 33.5 % to 48.3 % at 14-W output owing to the reduction of the switching loss of the MOSFET.

The proposed method is very effective to drive the MOSFET with a large parasitic capacitance. Particularly, if multiple MOSFETs are connected in parallel to enhance the current rating, the method is more suitable to such higher power applications.

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