Current-Doubler Based Multiport DC/DC Converter with Galvanic Isolation

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***Abstract*-This paper proposes a novel topology of a multiport DC/DC converter composed of an H-bridge inverter, a high-frequency galvanic isolation transformer, and a combined circuit with a current-doubler and a buck chopper. The topology has lower conduction loss by multiple current paths and smaller output capacitors by means of an interleave operation. Results of computer simulations and experimental tests show proper operations and feasibility of the proposed strategy.**

I. INTRODUCTION

In recent years, global-scale problems on environmental population have been increasing; hence, the effective reduction of the energy consumption is focused on. As solutions of the problems, there are usage of sustainable energy and vehicles driven by the energy. One of the most important factors of these solutions is energy conversion systems because the power generated by the sustainable energy resources and the power needed by loads are different [1]-[5]. However, in the current state, the energy sources, the storages, and the loads are connected to independent converters since such converters have only a single input-output. These lead a matter which is larger size of equipment. As a method to solve the matter, multiport converters are focused on [6]-[10]. In this paper, the multiport converter is applied to a small-scale battery DC power supply system.

The system using a higher-voltage source for high-power load is a recent technical trend to achieve smaller size. On the other hand, a low-power supply is still in demand at the same time. A DC power supply system which outputs mixed multiple voltages is required for these reasons. In the case, a small DC/DC converter which outputs different voltages is expected because using multiple DC/DC converters leads to larger size and higher cost.

In this paper, a new topology of the multiport DC/DC converter which has potential of smaller size and lower cost is proposed. The proposed topology is preliminary examined both computer simulations and experiments. The results prove feasibility of the proposed strategy. Chapter II explains proposed circuit configuration and operation principle, and chapter III indicates computer simulation conditions and results of the circuit. Preliminary experimental setup and test results are shown in chapter IV, and then chapter V indicates configuration and test conditions for main experiment which is in progress of making. Chapter VI describes simulation conditions and some results for the circuit of the main experiment. Finally, the conclusion is given in chapter VII.

II. PROPOSED CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

A. Configuration of Main Circuit and Controller

Fig. 1 shows a circuit diagram of the proposed topology. Multiport function is achieved by adding S5, S6, L3 and L4 to an isolated DC/DC converter based on a current-doubler.

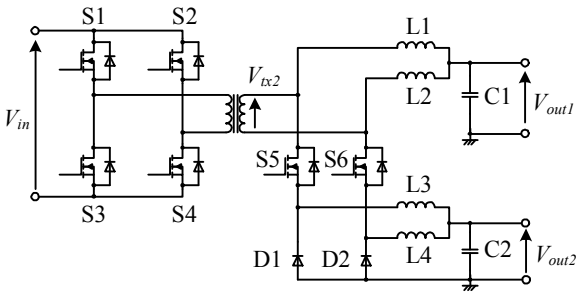
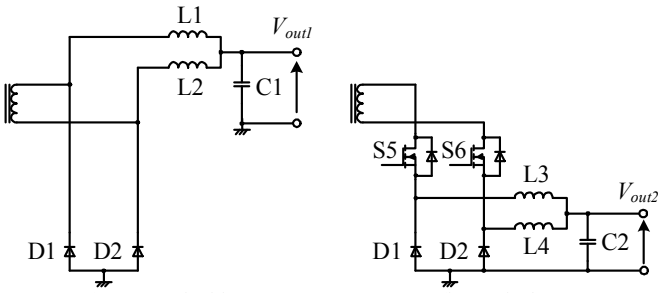


Fig. 1. Proposed dual port DC/DC converter.



(a) Current doubler. (b) Buck chopper.

Fig. 2 Decomposed configuration of secondary circuit.

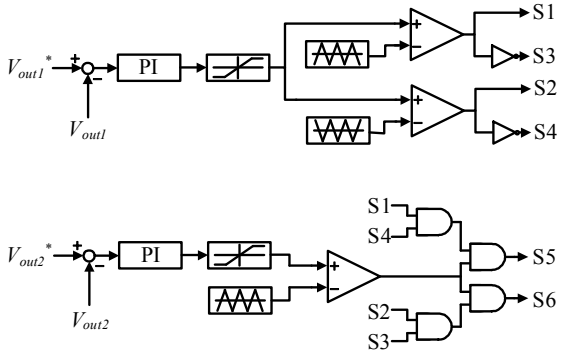


Fig. 3. Block diagram of proposed circuit controller.

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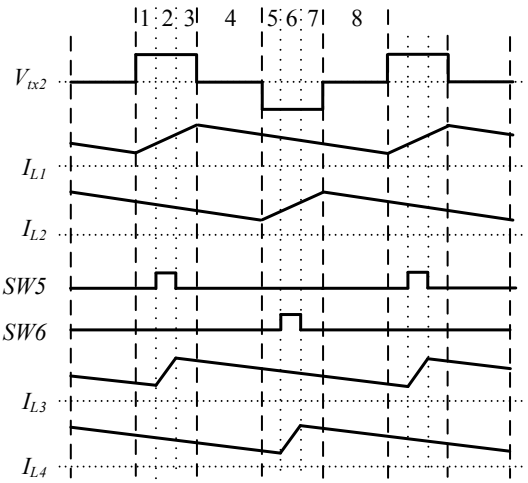


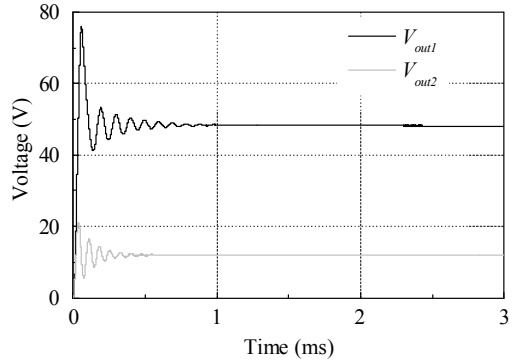
Fig. 4. Operation modes of proposed dual port DC/DC converter.

The primary side is an H-bridge inverter connected through a high-frequency transformer to the secondary side. The secondary circuit is a combination of the current-doubler composed of S7, S8, L1 and L2 (Fig. 2 (a)) and a buck chopper composed of S5, S6, D1, D2, L3 and L4 (Fig. 2 (b)). The circuit is characterized by having one inverter, one transformer and outputting two different voltages. D1 and D2 are shared by the both circuits, which makes the component counts lower. Fig. 3 shows a block diagram of the proposed circuit controller. V_{out1}, which is a voltage of the output 1 is controlled by pulse width control (PWC) of the primary inverter (S1 to S4), while V_{out2} which is a voltage of output2 is controlled by S5 and S6 in the secondary circuit. The command values of V_{out1} and V_{out2} are 48 V and 12 V, respectively. In this paper, it is defined that an output of the current-doubler is "output 1" and an output of the buck chopper is "output 2."

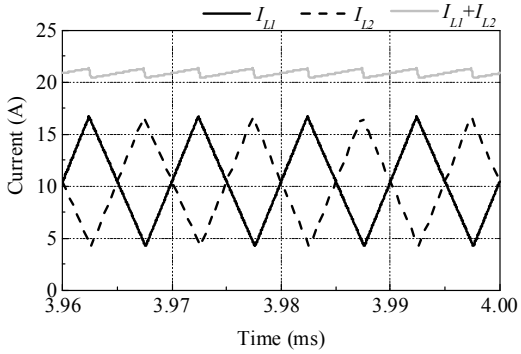
B. Circuit Operation

Fig. 4 shows eight operation modes of the secondary circuit. In the figure, it is hypothesized that the primary circuit generates a three-level output to the transformer. V_{tx2} is a voltage between both terminals of the secondary side of the transformer. While V_{tx2} is positive and SW5 is turned off, L1 is charged by the electromotive force of the transformer, and L3 discharges to the output 2 (modes 1 and 3). While V_{tx2} is positive and SW5 is turned on, the electromotive force of the transformer charges not only L1 but also L3. While V_{tx2} is zero and negative, the energy charged in L1 and L3 is discharged to each output (modes 4 and 8). While V_{tx2} is negative and SW6 is turned off, L2 is charged by the electromotive force of the transformer, and L4 discharges to the output 2 (modes 5 and 7). While V_{tx2} is negative and SW6 is turned on, L4 is also charged by the electromotive force of the transformer energy (mode 6). While V_{tx2} is zero or positive, the energy charged in L2 and L4 are discharged to each output (modes 4 and 8).

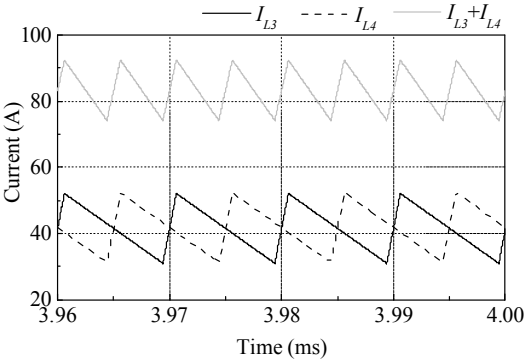
As shown in Figs. 1 and 2, the secondary circuit has double current paths to each output, where one is L1 and L2 paths,



(a) Output voltage waveforms.



(b) Inductor currents and their synthesized current of output 1.



(c) Inductor currents and their synthesized current of output 2.

Fig. 5. Dual port output voltage and inductor current waveforms.

and the other is L3 and L4 paths. This means that the proposed topology has a half conduction loss compared with the case of a single current path. In addition, the proposed topology has a two-phase interleave mode because of an AC rectangular wave from the transformer; thus, the capacitance values of the output capacitors C2 and C3 can be small. Applying a multiphase inverter makes it possible to increase the current paths, resulting in the lower conduction loss and the lower capacity of C2 and C3. With increasing the current paths, the components counts also increase. On the other hand, the current capacity and each component size become lower. This leads higher space occupancy rate of the circuit package by flexible implementation. For this reason, the proposed topology has potential of higher power density.

By employing the synchronous rectification system using MOSFETs instead of D1 and D2, the proposed topology achieves higher power density with lower losses. Therefore,

TABLE I.
SIMULATION PARAMETERS.

Parameters	Values
Switching Frequency	100 kHz
V_{in}	400 V
V_{out1}	48 V
V_{out2}	12 V
R1	2.3 Ω
R2	0.14 Ω
L1 and L2	20 μH
L3 and L4	5 μH
C1	47 μF
C2	94 μF

TABLE II.
PRELIMINARY EXPERIMENTAL TEST PARAMETERS.

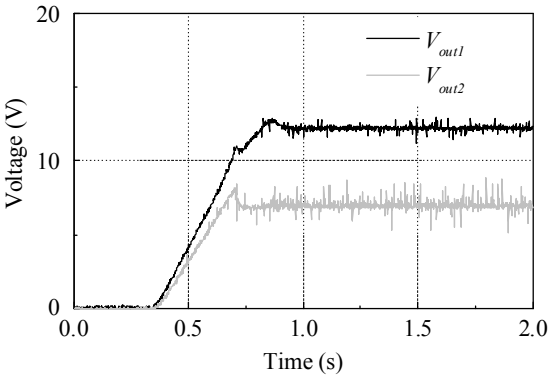
Parameters	Values
Switching Frequency	100 kHz
V_{in}	80 V
V_{out1}	12 V
V_{out2}	6 V
R1	1.8 Ω
R2	1.8 Ω
L1 and L2	20 μH
L3 and L4	5 μH
C1	47 μF
C2	94 μF

it is considered that the proposed topology contributes smaller size and lower cost of the DC/DC converter.

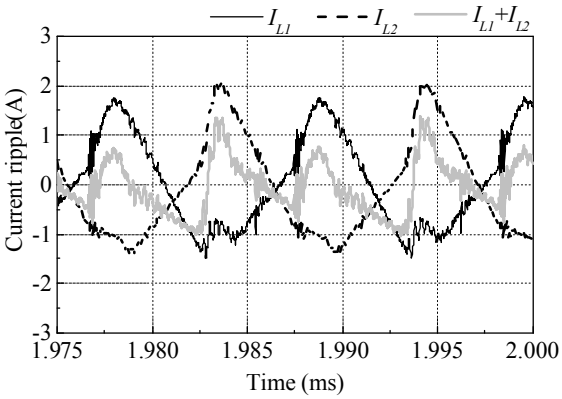
III. PRELIMINARY COMPUTER SIMULATIONS FOR CONFIRMING OPERATION PRINCIPLE

TABLE I shows computer simulation conditions. V_{in}, V_{out1}, and V_{out2} are chosen from voltages assumed for automotive applications. R1 and R2 are determined so that each output power rating is 1000 W. L1 to L4 have enough values to prevent the current ripple from getting high, and C1 and C2 also have enough values to suppress output ripples.

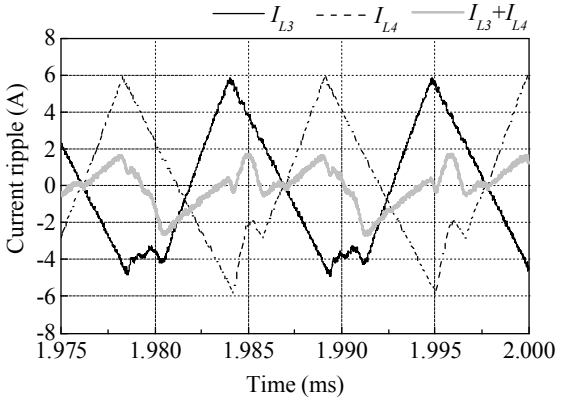
Fig. 5 shows the simulation results. Fig. 5 (a) indicates two-output voltage waveforms controlled stably in the steady state within 1 ms. Although an overshoot appears before the steady state, it is considered that the overshoot can be suppressed by adopting suitable controlled parameters. Fig. 5 (b) shows the currents of L1, L2, and the synthetic both currents, and Fig. 5 (c) shows the currents of L3, L4, and the synthetic both currents. As can be seen in the figures, the interleaved currents are confirmed, and the synthetic current ripple is effectively reduced with doubling the ripple frequency, especially in Fig. 5 (b). These results show that the proposed circuit works with expected principle.



(a) Output voltage waveforms.



(b) Inductor current ripples and their synthesized current ripple of output 1.



(c) Inductor current ripples and their synthesized current ripple of output 2.

Fig. 6. Output voltage and inductor current waveforms obtained in preliminary experimental.

IV. PRELIMINARY EXPERIMENTAL SETUP AND TEST RESULTS FOR VERIFICATION OF OPERATION

In order to confirm the validity of the proposed technique, several preliminary tests have been conducted with a scale-down experimental setup. TABLE II shows the preliminary test conditions. V_{in} is one-fifth, V_{out1} is one-fourth, and V_{out2} is half of the final prototype in the simulation. R1 and R2 are chosen so that the output power of V_{out1} is 80 W and that of V_{out2} is 20 W.

Fig. 6 shows the test results. Fig. 6 (a) is V_{out1} and V_{out2} waveforms. These are controlled stably in the steady state without significant overshoot. V_{out1} and V_{out2} are controlled to

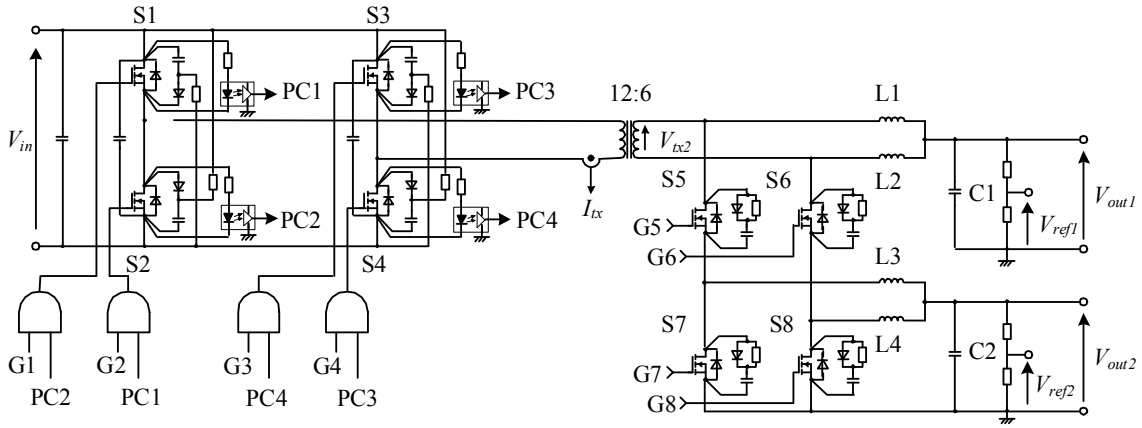


Fig. 7. Whole system configuration of proposed dual port DC/DC converter for final prototyping.

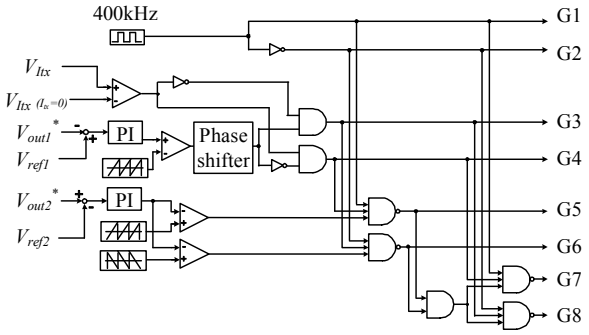


Fig. 8. Control block diagram of dual port DC/DC converter for final prototyping.

be 12 V and 6 V, respectively. It takes approximately 0.5 s to reach the steady state after turning on the circuit. The time to be steady state should be shortened by choosing proper control parameters. During the steady state, both output voltages have high-frequency noises. It is considered that the noises are caused by resonance of parasitic inductance and capacitance. The noises should be removed by making the circuit layout appropriate with lower parasitic circuit parameters and putting low-pass filters in suitable locations.

Fig. 6 (b) shows current ripples of L1, L2, and the synthetic current. The ripples of L1 and L2 are 3.2 A and 3.4 A, respectively, and the synthetic current ripple is 2.3 A. Fig. 6 (c) shows the same waveforms of L3, L4, and the synthetic current. The ripples of L3 and L4 are 10.9 A are 12 A, respectively, and the synthetic current ripple is 4.6 A. In the both figures, periodical noises are observed in convex downward part of each current. It is considered that the noises are caused by the reverse voltages of S5 and S6. The noises also come from the parasitic elements same as the high-frequency noises.

As well as the simulation results, the test result indicates that the two different output voltages are properly controlled as expected, interleaved currents are confirmed, and the synthetic current ripples are effectively reduced with doubling the ripple frequency. These results show that the proposed circuit works with actual circuit.

TABLE III.
Parameters of proposed dual port DC/DC converter.

Parameters	Values
Switching Frequency	400 kHz
V_{in}	400 V
V_{out1}	48 V
V_{out2}	12 V
R1	2.3 Ω, 23 Ω
R2	0.14 Ω, 1.4 Ω
Transformer turn ratio	N1 : N2 = 12 : 6
L1 and L2	2.5 μH
L3 and L4	1 μH
C1	44 μF
C2	141 μF

V. WHOLE SYSTEM CONFIGURATION AND TEST CONDITIONS FOR FINAL PROTOTYPE

It is confirmed that the preliminary circuit was operated as expected principle. In this chapter, a circuit, a control block diagram, and test conditions for main test are indicated.

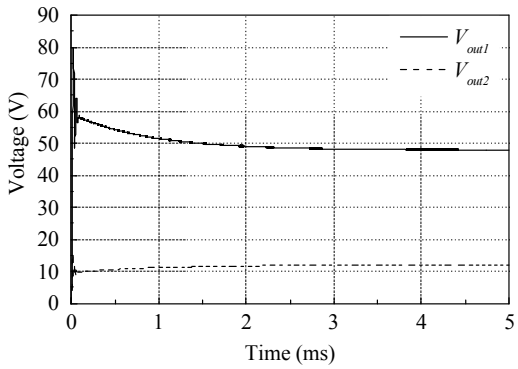
Figs. 7 and 8 show the circuit diagram and a block diagram of the circuit controller. Instead of diodes, MOSFETs are employed (S7 and S8 in Fig. 6). The controller generates G1 to G8 signals which are gate signals of S1 to S8. G1 is a 50-% duty cycle 400-kHz rectangular wave, and G2 is an inverted signal of G1. G3 is a phase-shifted signal based on G1, and G4 is an inverted signal of G3. An optocoupler is put in each MOSFET of the primary side to detect the drain-source voltages (PC1 to PC4). These signals are input to interlock circuit to make proper dead times of the H-bridge inverter. A corresponding voltage to the transformer current (V_{Itx}) and $V_{Itx(Itx=0)}$, which is a voltage when V_{Itx} = 0 are also needed to the proper switching of S3 and S4. G5 and G6 are changed by situations of G1 to G4. G7 and G8 are also decided by situations of G1 to G6.

TABLE III indicates experimental parameters. Switching frequency is 400 kHz so that size of passive components gets smaller. R1 and R2 values are chosen through the situations of the load change tests which are 100 % and 10 % of the load power. When the load power is 100 %, both output powers are 1000 W. The transformer turn ratio is 12 : 6, which is considered that the inverter part and the transformer part and the current-doubler part have equable voltage transformation ratio when load power is 100 %. L1 to L4, and C1 and C2 are determined so that the total size of these passive components is reduced. The values listed in TABLE III have not appropriately tuned yet, and the optimal values are currently investigated while the final prototyping is done.

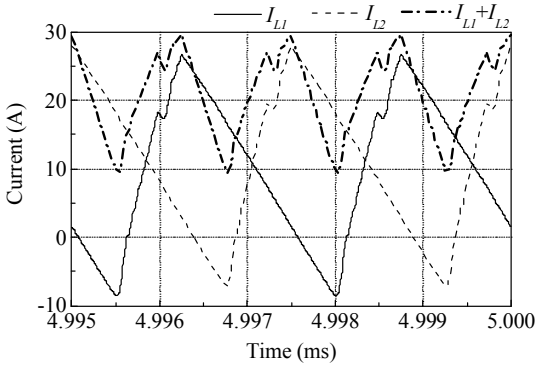
VI. COMPUTER SIMULATIONS FOR FINAL PROTOTYPING

Fig. 9 indicates the simulation results for the experimental tests. Fig. 9 (a) shows the output voltage waveforms. The two output voltages are controlled stably in the steady state. V_{out1} takes approximately 4 ms to be steady state and V_{out2} takes approximately 3 ms to be stable. Overshoots are observed in the both waveforms. Particularly, V_{out2}'s overshoot is more than 30-V higher than the command value (48 V). These overshoots are led by control parameters. The parameters should be tuned from the viewpoints of the overshoots and the waveform behavior when the load changes.

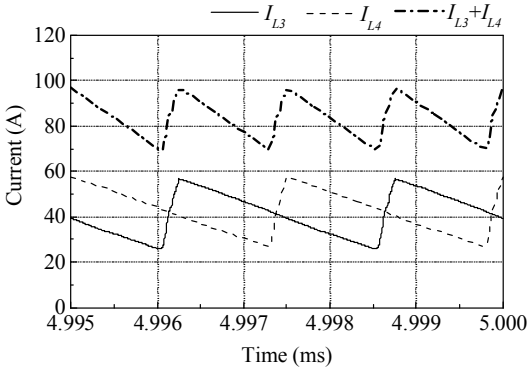
Fig. 9 (b) shows currents of L1, L2, and the synthetic current. Each current has some periodical noise in convex upward part of each current. This noise is caused by the reverse voltage of S5 and S6 as well as the waveforms of Fig. 6 (b). Since the operation modes of the experimental tests are changed from that of the preliminary experimental tests, the points where the noises appear are different between Fig.6 (b) and Fig. 9 (b). Fig. 9 (c) shows currents of L3, L4, and the synthetic both currents. The noises from the reverse voltage of S5 and S6 are also shown although these are small. It is because current values are much higher than the noises. In Figs. 9 (b) and (c), it is confirmed that the currents are interleaved and the synthetic current ripple is effectively reduced by doubling the ripple frequency.



(a) Output voltage waveforms.



(b) Inductor current ripples and their synthesized current ripple of output 1.



(c) Inductor current ripples and their synthesized current ripple of output 2.

Fig. 9. Experimental output voltage and inductor current waveforms.

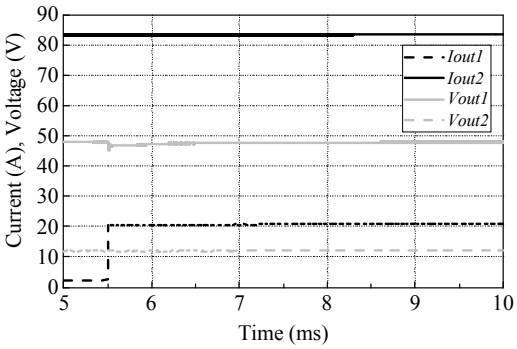
Fig. 10 indicates that results of load change tests. When time is 5.5 ms, load factors are changed. Figs. 10 (a) and (b) show that the load power of the both outputs is changed from 10 % to 100 %. Figs. 10 (c) and (d) show that load factors of both outputs are changed from 100 % to 10 %. In Fig. 10 (a), when I_{out1} are changed from 10 % to 100 %, V_{out1} swings down 4 V and it takes approximately 4 ms to get back to the steady state. On the other hand, V_{out2} and I_{out2} do not change at all. Fig. 10 (c) shows similarly results to Fig. 10 (a). When I_{out1} are changed from 100 % to 10 %, V_{out1} swings up 4 V and it takes 4 ms to get back to the steady state. On the other hand, V_{out2} and I_{out2} do not change at all. These results imply that the voltage and current of output2 are not affected by the load change of output1. Fig. 10 (b) shows that when I_{out2} are changed from 10 % to 100 %, I_{out2} has 3-A overshoot and V_{out2} little changes. In addition, I_{out1} swings down 3 A, and V_{out1} also swings down 7 V. It takes more than 3 ms for these waveforms to get back to the steady state. Fig. 10 (d) shows similarly results to Fig. 10 (b). Fig. 10 (d) also indicates that when I_{out2} are changed from 100 % to 10 %, V_{out2} seldom changes. At the same time, I_{out1} swings up 3 A, and V_{out1} also swings up 5 V. It takes more than 3 ms to get back to the steady state. According to the results, it is considered that the voltage and the current of the output 1 are affected by the load change of output 2 in contrast to the case when the load change of the output 1.

It is considered that there are two reasons why the waveforms of the output 1 are affected by the load change of the output 2, and the waveforms of the output 2 are not affected by the load change of the output 1. One is because the current variation range of I_{out2} is wider than that of I_{out1}. It means that although the output 2 is actually affected by the

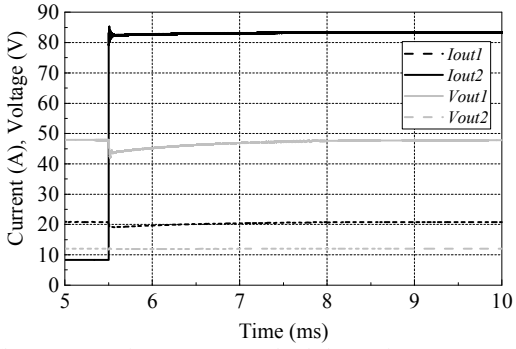
load change of the output 1, it could not be observed because of a narrow current variation range of I_{out1}. Another reason is because deference of complexity of the control system between V_{out1} and V_{out2}. A function of S1 to S4 is power transport from input source to the transformer including a control of V_{out1}. It means that S1 to S4 also supply power to V_{out2} although they do not control V_{out2}. On the other hand, S5 and S6 operate to control V_{out2} acting as a buck chopper. It means that S5 and S6 just chop and control the power from the transformer. Therefore, the output 2 waveform is not affected by the load change of the output 1 because the waveforms of the output 2 are compensated by S5 and S6, when the load of the output 1 is changed. In contrast, the output 1 waveform is affected by the load change of the output 2 because when the load of the output 2 is changed, operation of adjusting supply power to V_{out2} disturbs to keeping V_{out1} stable. To keep independence of the both outputs, it is considered that the control link between the inverter, S5, and S6 should be optimized.

VII. CONCLUSION

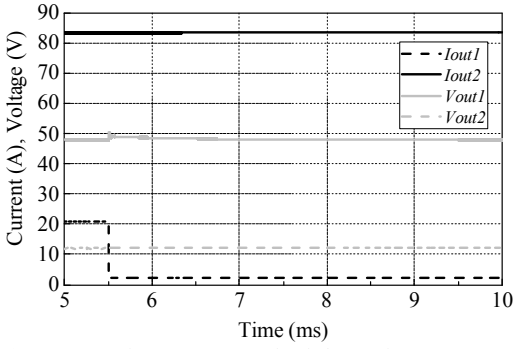
In this paper, a novel topology of the current-doubler based multiport DC/DC converter has been proposed and been investigated. The secondary circuit has a mixed structure composed with a current-doubler and a buck chopper, which effectively reduces the conductive loss and equipment size. The simulation results and preliminary experimental test results has proven feasibility of the proposed approach. The experimental test results of the final prototype will be demonstrated in the very near future work.



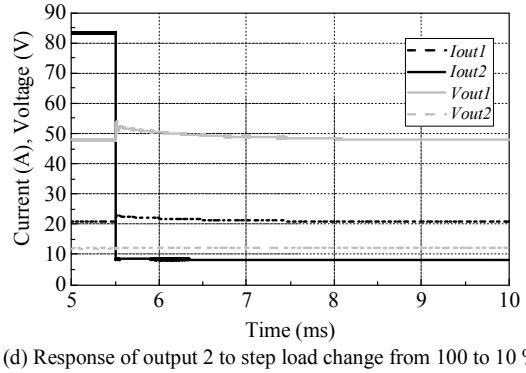
(a) Response of output 1 to step load change from 10 to 100 %.



(b) Response of output 2 to step load change from 10 to 100 %.



(c) Response of output 1 to step load change from 100 to 10 %.



(d) Response of output 2 to step load change from 100 to 10 %.

Fig. 10. Responses of dual ports to step load change.

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