Space Vector Modulation of Dual-Inverter System Focusing on Improvement of Multilevel Voltage Waveforms

Yoshiaki Oto, Toshihiko Noguchi, *Senior Member, IEEE*, Takanari Sasaya, Takahiro Yamada, and Ryoya Kazaoka

***Abstract*—A space vector modulation (SVM) technique of a dual-inverter system for an open-end winding motor drive is described in this paper, where one inverter has a battery power source and the other has an only capacitor across the dc bus. The SVM must be achieved to operate the motor with field-oriented control and simultaneously to control the capacitor voltage at a constant value by using redundant switching states of the dual-inverter system. The control of the capacitor voltage is carried out by selecting a charging or a discharging mode in each redundant switching state, taking the instantaneous motor power factor into account. In addition, it is also required to reduce the error voltage pulses, which are generated in output multilevel voltage waveforms during the dead time. The compensation method of the existing dead-time scheme and the improved SVM sequence to reduce the error voltage vectors are proposed in this paper. The proposed methods are examined through several experimental tests and are confirmed to generate superior output voltage waveforms from the viewpoint of the measured total harmonic distortion and *dv/dt*.**

***Index Terms*—Capacitor voltage control, dead time, dual-inverter system, open-end winding motor, space vector modulation (SVM).**

I. Introduction

IN RECENT years, the focus of researchers has been on mileage improvement and autopilot techniques, aiming at further reduction of carbon dioxide emission of hybrid vehicles. Many of the current hybrid vehicles are based on the combination of a bidirectional chopper and a two-level inverter and drive a high-voltage permanent magnet (PM) motor. Therefore, the line-to-line voltage of the motor is a three-level waveform with the high *dv/dt*, which may cause deterioration of the total harmonic distortion (THD), conduction noise, and radiation noise [1]–[11]. The current system also has a drawback from a viewpoint of a failsafe because the motor can no longer be operated if either the chopper or the inverter is failed. Therefore, a dual-inverter system driving an open-end winding PM motor by two two-level inverters has been focused [12]–[16]. So far, the system with the 2:1 dc-bus voltage ratio has been studied to generate multilevel voltage waveforms to the motor [17], [18]. In addition, a dual-inverter system, where the dc-bus battery power source of one inverter is replaced with a capacitor, has also been studied to reduce the inverter power source [19]–[24]. In the case, it is required both to generate the multilevel voltage waveforms to the motor and simultaneously to control the capacitor voltage at a constant value with the space vector modulation (SVM). Particularly, it is indispensable to take an instantaneous motor power factor into account to control the charging or discharging modes of the capacitor [25]. However, the output multilevel voltage waveforms contain a lot of unexpected error voltage pulses during a dead time [26]. The dual-inverter system, where both inverters have a battery power source across the dc bus, has no error voltage pulses because the SVM can be implemented without taking capacitor voltage control into account [12], [13], [18]. Even for the dual-inverter system where one inverter has the capacitor across the dc bus, the error voltage pulses cannot be observed on the condition of a low sampling frequency because the error voltage pulses are generated during the dead time [23]. The method to reduce the error voltage pulses is introduced in the literature [27]; however, the existing method focuses only on the condition of a low modulation index, and a fluctuation of the switching speed due to the motor line current is not considered [28].

In this paper, the SVM for the dual-inverter system, where one of the inverters has the only capacitor across the dc bus instead of the battery power source, is described. The studied system can generate the multilevel voltage waveforms across the open-end winding terminals of the motor and simultaneously can regulate the capacitor voltage taking the instantaneous motor power

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Y. Oto and T. Noguchi are with the Department of Electrical and Electronics Engineering, Faculty of Engineering, Shizuoka University, Hamamatsu 432-8561, Japan (e-mail: ohto.yoshiaki.15@shizuoka.ac.jp; noguchi.toshihiko@shizuoka.ac.jp).

T. Sasaya, T. Yamada, and R. Kazaoka are with the Advanced Research and Innovation Center, Electronics R&I Division, Power Electronics R&I Department, Denso Corporation, Nisshin 470-0111, Japan (e-mail: takanari_sasaya@denso.co.jp; takahiro_t_yamada@denso.co.jp; ryoya_kazaoka@denso.co.jp).

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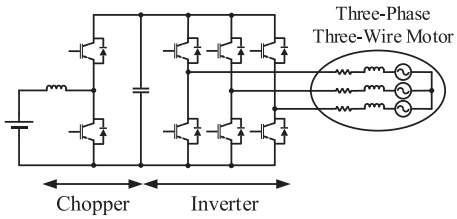

Fig. 1. Conventional motor drive system of hybrid vehicles.

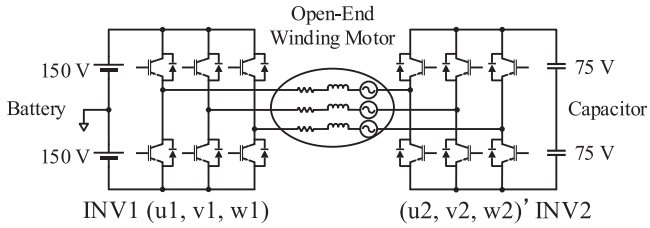

Fig. 2. Studied motor drive with a dual-inverter system.

factor into account. In addition, the compensation method of the existing dead-time scheme and the improved SVM sequence to reduce the error voltage pulses are proposed in this paper. The proposed methods are examined through several experimental tests and are estimated with the measured THD and *dv*/*dt* results.

II. Configuration of the Dual-Inverter System

A. Circuit Configuration of the Dual-Inverter System

Fig. 1 shows a circuit diagram of the conventional system composed of a single two-level inverter driving a three-phase PM motor with a neutral point inside of the motor. Fig. 2 shows the studied dual-inverter system driving an open-end winding PM motor, where one inverter on the left-hand side is called INV1 and the other on the right-hand side is called INV2, whose dc-bus power source is replaced with a capacitor. Each leg of the both inverters is complementarily operated, and the combination of the switching states is expressed as (u1, v1, w1) (u2, v2, w2)′, where the switching states "1" and "0" mean that the upper arm is turned ON and OFF, respectively.

The dual-inverter system can generate the multilevel voltage waveforms by adding/subtracting one inverter voltage to/from the other inverter voltage. The multilevel voltage waveform generation is expected to improve the THD resulting in the copper loss and iron loss reductions and is expected to reduce the conduction and the radiation noises owing to the reduction of *dv*/*dt*. There is no common-mode voltage because the dc buses of the two inverters are not common. The system has a drawback of increasing the inverter counts and their dc-bus power source counts compared with the conventional single-inverter system. However, the system does not require any voltage boost power converter such as the bidirectional chopper.

There is a redundancy in the switching states of the dual-inverter system. In other words, a particular voltage vector can be applied to the motor by using different switching states, which makes it possible to operate the motor with controlling the capacitor voltage of INV2. The studied dual-inverter system,

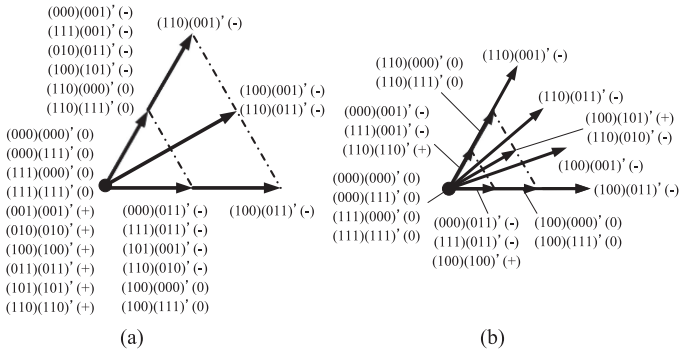

Fig. 3. Output voltage vector and capacitor charging or discharging mode of each switching state. (a) Dual inverter with a 1:1 dc-bus voltage. (b) Dual inverter with a 2:1 dc-bus voltage.

where the dc-bus battery across one of the inverter dc buses is replaced with the capacitor, can reduce the dc-bus power source counts; however, it reduces the fault-tolerant capability of the system. The existing dual-inverter system, where two inverters have the battery power source, can continue to drive the motor even if one inverter dc-bus power source or one switching device of either inverter is failed. On the other hand, the studied system can continue to drive the motor only in the case of the failure of the inverter, which has the capacitor across the dc bus. From this point of view, the proposed technique can enhance the fault-tolerant capability of the conventional dual-inverter system with a dual-dc-bus battery source.

B. DC-Bus Voltage Ratio and Switching State Redundancy

The dual-inverter system discussed in this paper controls the INV2 capacitor voltage at a half value of the INV1 battery voltage. The reason is, in addition, to generate the nine-level voltage waveform to utilize the switching state redundancy for simultaneous control of the capacitor voltage and the multilevel voltage waveform generation with the SVM.

The single inverter can output eight voltage vectors, in which six are nonzero-voltage vectors and two are zero-voltage vectors. The output voltage vectors of the dual-inverter system are the total number of the output voltage vectors of the two inverters. Fig. 3 illustrates the output voltage vectors from 0° to 60° of the two dual-inverter systems, whose dc-bus voltage ratios are 1:1 and 2:1, respectively. In the figure, the capacitor charging, holding, and discharging modes are noted as "+," "0," and "−" after the switching states, respectively. As shown in Fig. 3, a particular voltage vector can be applied to the motor by using different switching states, which means that the both systems have switching state redundancy. In the case of the 1:1 dc-bus voltage ratio, however, only one of the capacitor charging or discharging modes is available among the redundant switching states; hence, it is impossible to switch over the charging mode and the discharging mode redundantly. On the other hand, the dual-inverter system with the 2:1 dc-bus voltage ratio has both the charging mode and the discharging mode in the redundant switching states to output a particular voltage vector. This makes it possible to achieve the capacitor voltage control and the

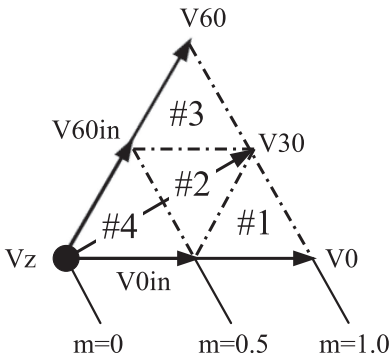

Fig. 4. Voltage vectors used in SVM and modulation index.

multilevel voltage waveform generation at the same time with the SVM, which is the reason why the 2:1 dc-bus voltage ratio has been employed for the studied dual-inverter system.

However, the longest voltage vectors that configure the most outer hexagon do not have the redundancy even if the 2:1 voltage ratio is employed, so the longest voltage vectors are not used in the SVM discussed in this paper. It means that the dc-bus battery voltage of INV1 in the studied dual-inverter system requires the same battery voltage as that of the conventional single two-level inverter in order to generate the same fundamental voltage to the motor. In other words, the studied system requires the dc-bus voltage ratio 450:225 in order to generate the same fundamental voltage as the conventional dual-inverter system, where two inverters have a battery source across both dc bus with the 300:150 dc-bus voltage ratio.

III. Selection of Voltage Vectors in the SVM

Fig. 4 illustrates the voltage vectors whose phase angle is from 0° to 60°, for example, where m denotes a modulation index. In this paper, the modulation index is defined as $m = 1.0$ when the circular locus of the voltage vector generated with the SVM is inscribed in the outer hexagon and as $m = 0.5$ when the locus is inscribed in the inner hexagon; in this case, it is possible to control the capacitor voltage with the redundant switching states. The system can output longer voltage vectors than $m = 1.0$ by using the longest voltage vectors, which configure the most outer hexagon, as shown in Fig. 3(b); however, the longest vectors do not have a switching redundancy, as described above, i.e., it cannot control the capacitor voltage with the SVM. Therefore, the modulation index $m = 1.0$ is defined, as shown in Fig. 4.

The SVM is carried out by synthesizing some discrete inverter voltage vectors at an optimal ratio to output a commanded voltage vector with an arbitrary norm and an arbitrary phase angle. The commanded voltage vector is generated by synthesizing three voltage vectors surrounding the commanded voltage vector in a triangular shape illustrated in Fig. 4. In the case of the commanded voltage vector in the #1 triangle sector, for example, the three voltage vectors V0, V0 in, and V30 surrounding the corresponding triangle sector are used for the SVM to synthesize the commanded voltage vector, which contributes to reduce the dv/dt of multilevel voltage waveforms. In the case of the commanded voltage vector in the triangle sectors from #1 to #3, zero-voltage vectors Vz cannot be used for the SVM, resulting in nine-level voltage waveforms across the open-end winding terminals. In the case of the triangle sector #4, Vz must be used resulting in five-level voltage waveforms.

IV. Capacitor Voltage Control

A. Capacitor Voltage Control of INV2

The dc-bus battery power source of INV2 is replaced with the capacitor in the studied dual-inverter system. The capacitor voltage of INV2 must be controlled to keep at a half of the dc-bus battery voltage of INV1 by charging and discharging it, simultaneously generating the multilevel voltage waveforms to the motor windings.

The dual-inverter system has switching state redundancy and can generate a particular voltage vector with several different redundant switching states, as described previously. The capacitor charging or discharging mode is decided according to the polarity of the current flowing into the capacitor in every switching state. As shown in Fig. 5, the multilevel voltage waveform generation with the SVM and the capacitor voltage control can simultaneously be carried out by selecting an optimal switching state among the redundant states, i.e., switching state charging or discharging the capacitor properly. The condition of almost unity power factor is assumed in Fig. 5.

B. Impact of the Instantaneous Motor Power Factor

Fig. 6 shows the relationship between the phase of the current vector and the polarities of the motor line currents, where the polarity signs indicate the motor line current directions, i.e., "+" means a direction from INV1 to INV2, while "–" means the opposite direction. The capacitor charging or discharging mode is determined by the motor line current direction in every switching state.

However, the PM motor that is connected to the dual-inverter system as a load is inherently an inductive load; thus, it is assumed that the phase of the line current vector lags behind the voltage vector generated to the motor windings with the SVM. Each line current direction changes according to the instantaneous motor power factor, which may be affected by the motor parameters and the motor operating conditions. This implies that the instantaneous motor power factor must be considered in order to control the capacitor voltage at a constant value. Let us assume that the commanded voltage vector is in the hatched sector, as shown in Fig. 6. The three voltage vectors V60, V60 in, and V30 surrounding the hatched sector are used to synthesize the commanded voltage vector. The maximum lagging phase angle between the voltage and the current vectors is 90°; thus, the current polarity is one of "B," "A," and "F." For example, the relationship between the redundant switching states and the capacitor charging or discharging mode of the voltage vector V30 is shown in Fig. 7. The switching state (110)(010)′ is the capacitor charging mode in the case of the current polarity "B," but the identical switching state is the capacitor discharging mode in the case of the "A" or "F." In general, the relationship cannot

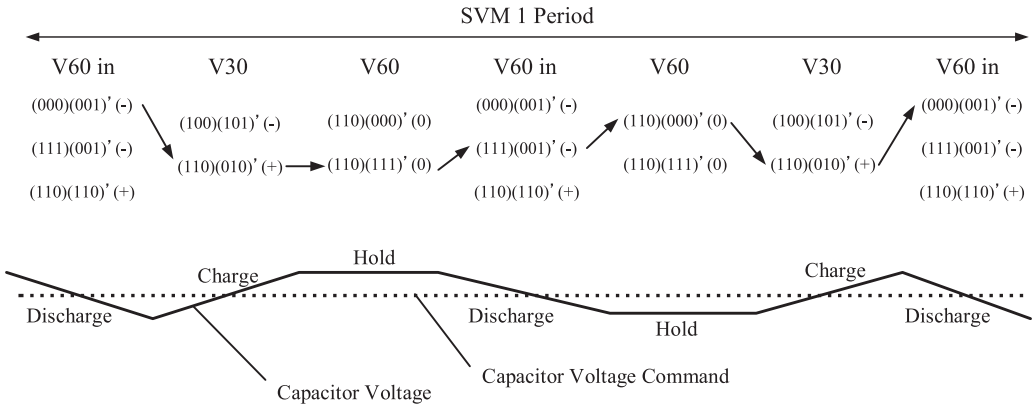

Fig. 5. Simultaneous control of capacitor voltage and multilevel voltage waveform generation with SVM.

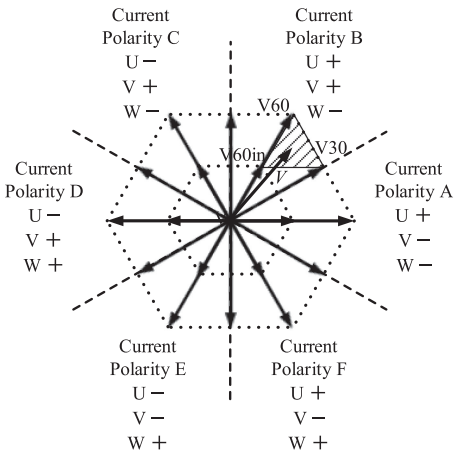

Fig. 6. Relationship between phase of current vector and directions of motor line currents.

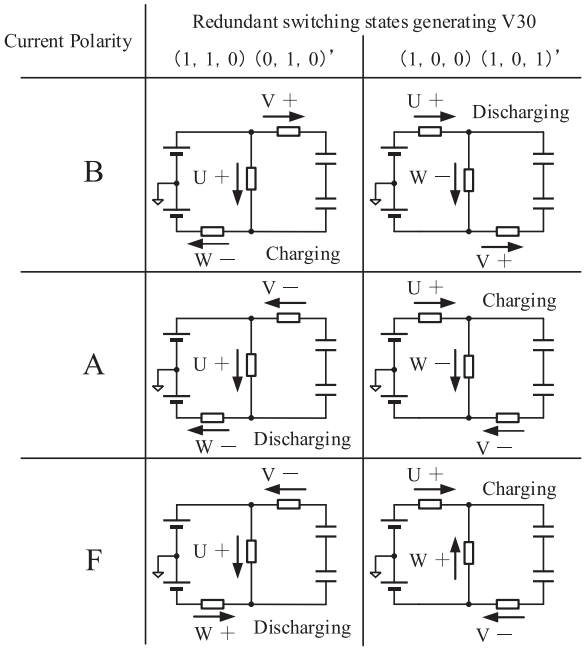

Fig. 7. Relationship between redundant switching states to output V30 and capacitor voltage control modes.

uniquely be determined because the phase of the motor line current vector changes due to the instantaneous motor power factor. In order to control the capacitor charging or discharging, it is indispensable for the SVM to select an appropriate switching state among the redundant switching states, taking the instantaneous motor power factor into account.

V. Computer Simulation and Results

Some computer simulations have been conducted to examine the basic operation of the dual-inverter system for the open-end winding PM motor drive, where only the capacitor is installed across the dc bus of INV2, and the SVM technique described above is employed. The control block diagram is shown in Fig. 8. The motor is controlled with a field-oriented control (vector control) algorithm, so there is a speed control loop and a current control loop in the controller. The phase angle between the voltage vector and the motor line current vector is calculated on the synchronously rotating (dq) reference frame, which is utilized to select the most appropriate switching state among the redundant switching states with the feedback value of the capacitor voltage of INV2. Table I shows the simulation conditions, and Fig. 9 shows the operation waveforms obtained through the simulations. The motor speed, the instantaneous motor power factor, the capacitor voltage, and the voltage across the U-phase winding terminals are shown from the top to the bottom of Fig. 9. Even though the instantaneous motor power factor is varied dynamically by a transient acceleration of the motor speed, the capacitor voltage is properly controlled at the command value 150 $\pm$ 5 V, and the five-level and nine-level voltage waveforms are observed at $m = 0.35$ and $m = 0.7$, respectively.

VI. Experimental Setup and Test Results

Experimental setup and experimental tests of the dual-inverter system have been conducted, as shown in Fig. 10. The details of the controller are shown in Fig. 11. The SVM is implemented in the digital signal processor (DSP), and the DSP generates the signals of output voltage vectors and the time duration of each switching state to the field-programmable gate array (FPGA).

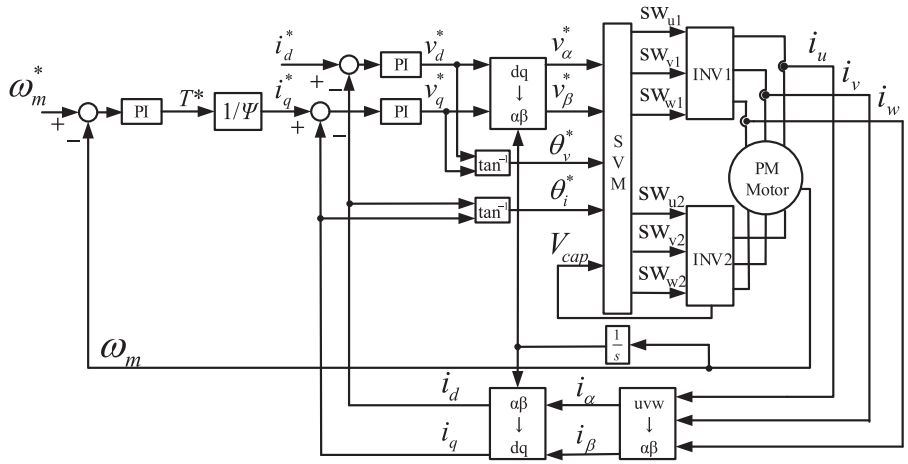

Fig. 8. Control block diagram of the dual-inverter system feeding an open-end winding PM motor.

TABLE I
COMPUTER SIMULATION CONDITIONS

Switching frequency		10 kHz
Voltage of battery (INV1)		300 V
Voltage of capacitor (INV2)		150±5 V
Capacitance of capacitor (INV2)		1329.4 μF
Motor speed command value		1000, 2000 r/min
Dead time		0 μs
Motor parameters	Number of poles	8
	Number of flux linkage	0.174 Wb
	Moment of inertia	0.00173 kgm^2
	Damping coefficient	0.005 N/rad/s
	Phase resistance	1 Ω
	Phase inductance	5 mH

The FPGA outputs the switching signals to each gate driver of INV1 and INV2. The open-end winding PM motor is controlled by a field-oriented control (vector control) algorithm, and its speed is regulated at 800 r/min ($m = 0.35$) and 1600 r/min ($m = 0.7$) by a load servo motor directly connected to the test motor. The rated output power of the test motor is 1 kW and is fed by the two 5-kVA inverters, where one of the inverters has the only capacitor across the dc bus and the capacitor is precharged at a half of the battery voltage across the other inverter dc bus. No extra circuit is required for precharging the capacitor because the proposed SVM algorithm with control of the capacitor voltage automatically precharges the capacitor in starting up the system. Experimental test conditions are shown in Table II, and the test results are shown in Fig. 12. The multilevel voltage waveforms are generated across the open-end winding terminals of the test motor, but the waveforms contain a lot of unexpected error voltage pulses, which deteriorate the THD of the multilevel voltage waveforms. The error voltage pulses are generated especially on the conditions of the capacitor charging mode at a low modulation index and the capacitor discharging mode at a high modulation index. However, the three-phase line currents are balanced, and the capacitor voltage is properly controlled at 150 V within the commanded hysteresis band.

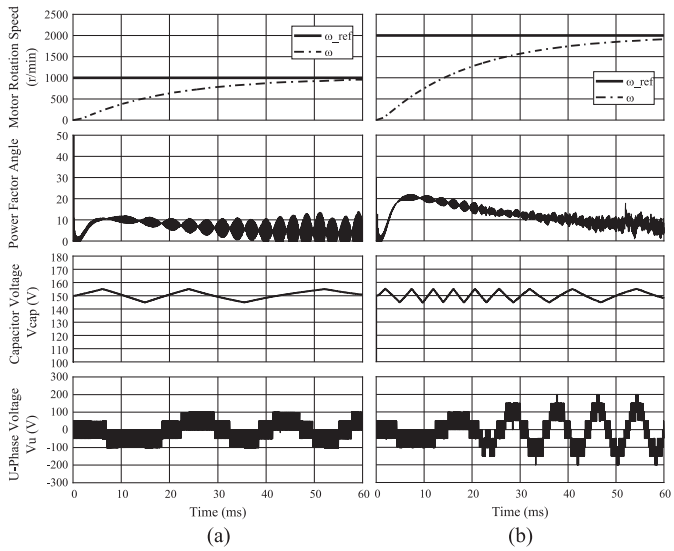

Fig. 9. Simulation results. (a) $m = 0.35$ (1000 r/min). (b) $m = 0.7$ (2000 r/min).

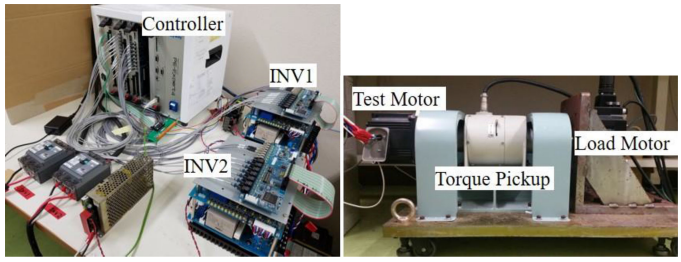

Fig. 10. Experimental setup of the proposed dual-inverter system.

VII. IMPACT OF THE DEAD TIME

A. Existing Dead-Time Scheme of the Dual-Inverter System

There are particular switching sequences in the SVM for the dual-inverter system, where the switching devices in the same phase of the both inverters are synchronously turned ON or OFF.

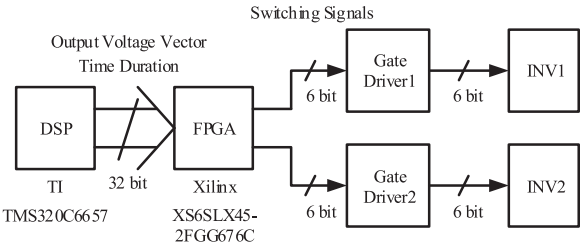

Fig. 11. Details of the controller.

TABLE II
EXPERIMENTAL TEST CONDITIONS

Switching frequency		10 kHz
Voltage of battery (INV1)		300 V
Voltage of capacitor (INV2)		150±5 V
Capacitance of capacitor (INV2)		1329.4 μF
d-axis current command value		0 A
q-axis current command value		3.7 A
Motor speed		800, 1600 r/min
Dead time		4 μs
Motor parameters	Number of poles	8
	Rated power	1000 W
	Rated speed	2000 r/min
	Rated torque	4.78 Nm
	Rated current	3.7 A
	Armature resistance	1.1 Ω
	Number of flux linkage	0.174 Wb
	d-axis inductance	11.0 mH
	q-axis inductance	25.0 mH

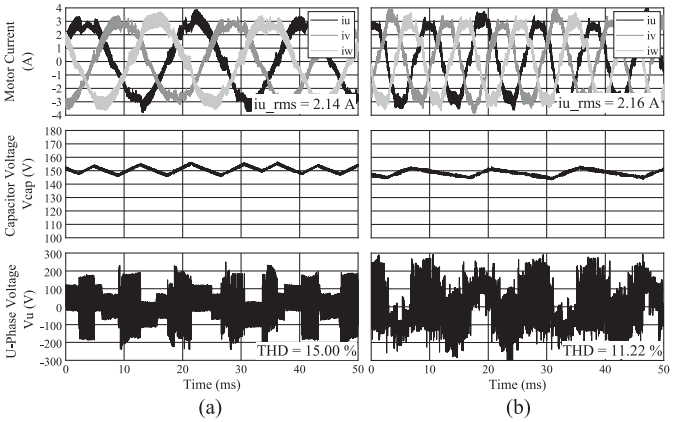

Fig. 12. Experimental test results. (a) $m = 0.35$ (800 r/min). (b) $m = 0.7$ (1600 r/min).

As shown in Fig. 13, for example, let us assume the transition from a switching state "A" to "B," where the upper arms of the both inverters are turned ON in "A," while the both lower arms are turned ON in "B." The switching states of INV1 and INV2 are, respectively, "0" and "1" during the dead time because the switching state during the dead time is determined by the motor line current direction. The unexpected error voltage vectors are

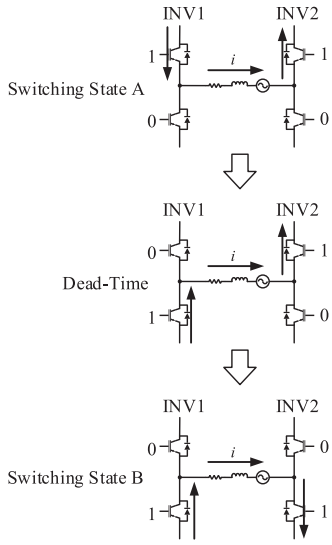

Fig. 13. Unexpected switching state in synchronous switching.

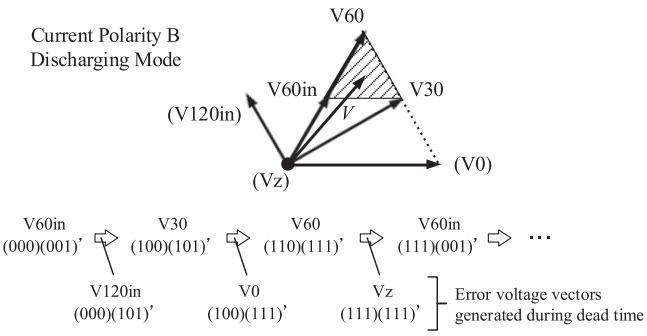

Fig. 14. Unexpected error voltages during dead time.

TABLE III
EXISTING DEAD-TIME SCHEME TO REDUCE ERROR VOLTAGES

State	INV1		INV2		Phase voltage
	Up	Un	Up	Un	
#1	1	0	1	0	Vdc1-Vdc2
#2	1	0	0	0	Vdc1-Vdc2
#3	0	0	0	1	0
#4	0	1	0	1	0

generated due to the unexpected switching states. In the case that the commended voltage vector is in the hatched sector of Fig. 14, the three voltage vectors V60, V60 in, and V30 are used for the SVM. The proper SVM sequence is V60 in → V30 → V60 → V60 in; however, the unexpected error voltage vectors such as V120 in, V0, and Vz are inserted during the dead time.

Table III shows the existing dead-time scheme for the dual-inverter system to avoid the unexpected error voltage vectors during the dead time. In the table, it is assumed that the line current direction is from INV1 to INV2. The upper arms of the both inverters are turned ON in state #1. In state #2, the first dead time is inserted in the inverter, where the line current flows into INV2. At that time, the upper arm of INV1 is kept turned

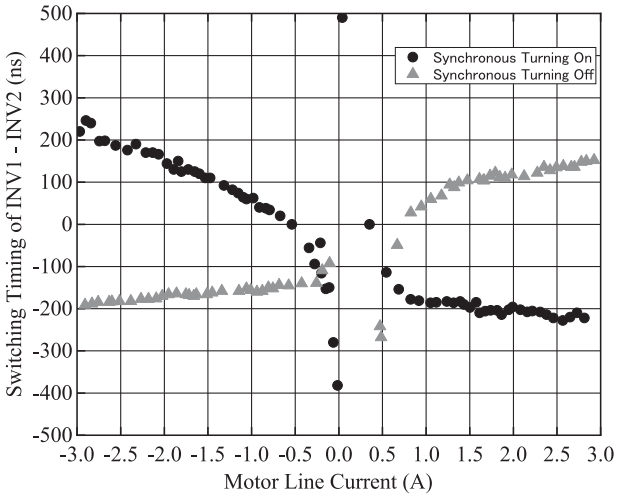

Fig. 15. Difference of switching speed between INV1 and INV2.

ON, and the upper arm of INV2 is also turned ON with the diode. Then, the second dead time is inserted in the other inverter (INV1) at the end of the first dead time, i.e., at the beginning of state #3. In state #3, the lower arm of INV1 is turned ON with the diode, which is during the second dead time, and the lower arm of INV2 is also turned ON, which is after the first dead time. In state #4, the lower arms of the both inverters are turned ON after the second dead time. In this way, the switching state is directly changed from INV1 is "1" and INV2 is "1" to INV1 is "0" and INV2 is "0", that is, the switching devices in the same phase of both inverters are synchronously turned ON or OFF without the unexpected switching state during the dead time.

B. Proposed Compensation of the Dead-Time Scheme

In fact, however, there is a difference of the switching speed in the same-phase switching devices of both inverters; hence, it is difficult to insert the second dead time precisely at the end of the first dead time. The measured difference of switching speed between INV1 and INV2 is shown in Fig. 15. In the figure, the positive line current indicates a direction from INV1 to INV2, and the negative line current does the opposite. It is required to compensate for the difference of switching transient time to reduce the error voltage vectors during the dead time. The compensation method is proposed in this paper, where a lookup table is made on the basis of Fig. 15 in advance, and the switching timing is adjusted according to the table by the FPGA, as there is no difference of the switching transient time.

Let us assume the synchronous turning OFF, as shown in Table III, where the turning-OFF time of the switching device of the INV1 upper arm is expressed as $t$off1, the turning-ON time of the switching device of the INV2 lower arm as $t$on2, and the reverse recovery time of the diode of the INV2 upper arm as $t$rr2. When the synchronous switching is done and the state changes from #2 to #3 in the existing dead-time scheme, the lower arm of INV1 is turned ON with the diode after the upper arm is turned OFF with the insulated-gate bipolar transistor (IGBT), while the lower arm of INV2 is turned ON with the IGBT after the upper arm is turned OFF with the diode. The switching transient time of INV1 is almost equal to the turning-OFF time of the IGBT

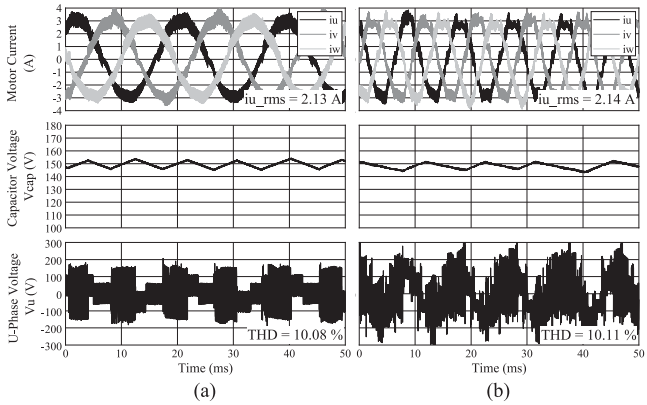

Fig. 16. Test results employing the existing dead-time scheme. (a) $m = 0.35$ (800 r/min). (b) $m = 0.7$ (1600 r/min).

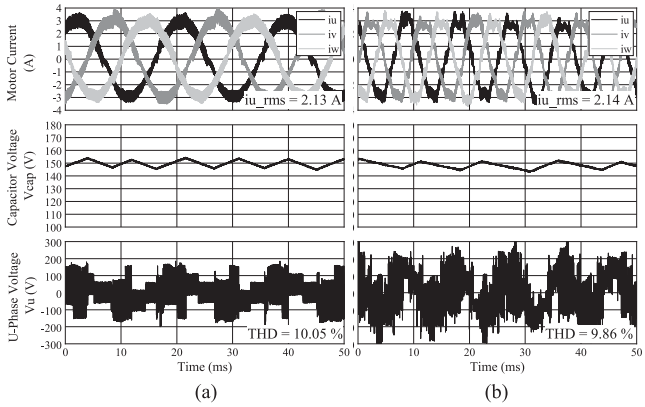

Fig. 17. Test results employing the proposed compensation. (a) $m = 0.35$ (800 r/min). (b) $m = 0.7$ (1600 r/min).

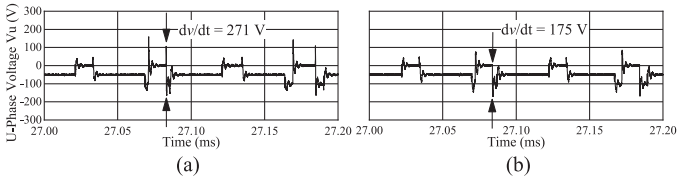

Fig. 18. Enlarged figure from 27.0 to 27.2 ms in test results at low modulation index. (a) Without the proposed compensation. (b) With the proposed compensation.

($t$off1) because the turning-ON time of the diode can be ignored for such a high speed, while the switching transient time of INV2 is the sum of the reverse recovery time of the diode ($t$rr2) and the turning-ON time of the IGBT ($t$on2), i.e., $t$rr2 + $t$on2. The switching transient time of INV1 is longer than INV2 in the case that the line current norm is small because the reverse recovery time of the diode of INV2 is shorter, i.e., $t$off1 > $t$rr2 + $t$on2. On the other hand, the switching transient time of INV1 is shorter than INV2 in the case that the line current norm is large, and particularly, the $t$rr2 is longer than the difference of $t$off1 and $t$on2, i.e., $t$off1 < $t$rr2 + $t$on2.

The test results employing the existing dead-time scheme and the proposed compensation are shown in Figs. 16 and 17, respectively. In addition, Fig. 18 shows enlarged figures of Figs. 16(a) and 17(a), i.e., the generated voltage waveforms at a low mod-

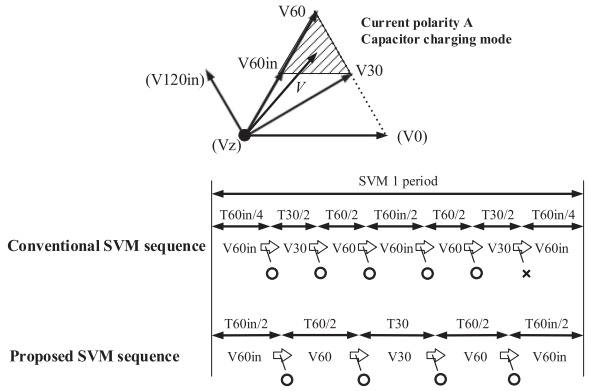

Fig. 19. Proposed SVM sequence.

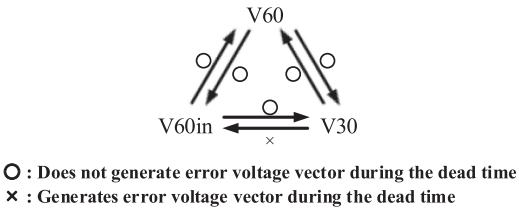

Fig. 20. Relationship between switching transitions and possibility to generate error voltage vectors during the dead time.

ulation index. As shown in Fig. 16, it is observed that the THD of generated voltage waveforms is reduced by 32.8% at a low modulation index ($m = 0.35$) and is reduced by 9.89% at a high modulation index ($m = 0.7$) with the existing dead-time scheme. The proposed compensation cannot reduce the THD remarkably, compared with the existing dead-time scheme, as shown in Fig. 17; however, it can reduce the *dv/dt* of a part of generated voltage waveforms by 35.4% especially at a low modulation index, as shown in Fig. 18. The reduction of the *dv/dt* is expected to reduce the conduction and radiation noises. All in all, it is observed that the existing dead-time scheme can reduce the THD of the generated multilevel voltage waveforms, and the proposed compensation technique can generate the superior voltage waveforms from the viewpoint of the *dv/dt*, compared with the existing scheme. The dead-time scheme is not so effective at a high modulation index because there is not only synchronous switching in the same phase of both inverters, but also complicated switching transients, where the switching devices in several phases in one inverter turn ON or turn OFF at the same time. For this reason, it is difficult to improve the generated multilevel voltage waveforms with the above dead-time technique at a high modulation index.

VIII. Proposed SVM Sequence

As shown in Fig. 19, for example, let us assume that the commanded voltage vector is generated in the hatched sector with the SVM on the condition of a high modulation index, current polarity A, and capacitor charging mode. In that case, the SVM sequence is composed of the three voltage vectors V30, V60, and V60 in. The possibility of the error voltage vectors during the dead time of every switching transition is shown in Fig. 20, where the switching transitions that do not

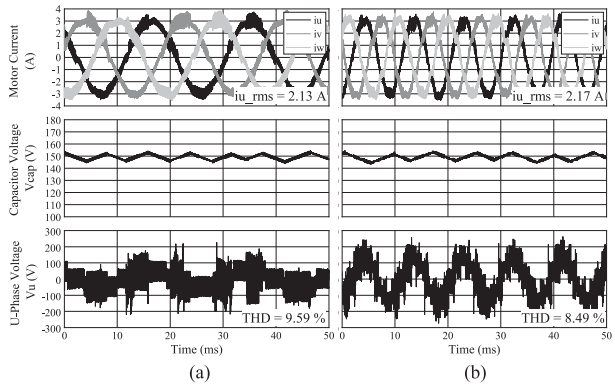

Fig. 21. Experimental test results employing proposed SVM technique. (a) $m = 0.35$ (800 r/min). (b) $m = 0.7$ (1600 r/min).

generate the error voltage vector during the dead time are noted as "○," and the opposite are noted as "×." Fig. 20 indicates that the error voltage vector is sure to be generated during the dead time of switching transition from V30 to V60 in even if the above dead-time techniques are employed.

The conventional SVM sequence, based on a general pulsewidth modulation sequence is composed, has seven states, as shown in Fig. 19. It means that the conventional SVM sequence is never achieved without the switching transition from V30 to V60 in, i.e., it cannot reduce the error voltage vectors at a high modulation index. On the other hand, the proposed SVM sequence has five states, that is, it is possible to compose the SVM sequence without the switching transition from V30 to V60 in, which generates the error voltage vector during the dead time, as shown in Fig. 19. The block diagram and the algorithm of the proposed SVM sequence are same as that of the conventional SVM sequence, based on which e.g., the capacitor charging or discharging mode of each switching state. The time duration of the output voltage vectors and the number of transitions in an SVM period are different from the conventional SVM sequence.

The test results of the dual-inverter system employing the above proposed SVM sequence are shown in Fig. 21. Compared with the conventional SVM sequence employing the existing dead-time scheme, it is observed that the THD is reduced by 5.11% at a low modulation index and is reduced by 16.0% at a high modulation index with the proposed compensation described previously and the proposed SVM sequence. The reduction of the THD of the generated voltage waveforms to the motor windings is expected to reduce the copper loss and the iron loss of the motor. Therefore, the proposed approach works well at both low and high modulation indexes.

IX. Conclusion

This paper described the SVM techniques of the dual-inverter system feeding an open-end winding PM motor, where the battery power source across one inverter dc bus is replaced with the capacitor. The SVM is achieved both to generate multilevel voltage waveforms across the open-end winding terminals and simultaneously to control the capacitor voltage constantly by selecting an optimal switching state among the redundant states, taking the instantaneous motor power

factor into account. It was also described in this paper that the unexpected error voltage pulses were generated in the output multilevel voltage waveforms during the dead time. The compensation method of the existing dead-time scheme and the improved SVM sequence were proposed and examined through several experimental tests in this paper. However, multilevel voltage waveforms still have the error voltage pulses, which will be investigated in detail in future works.

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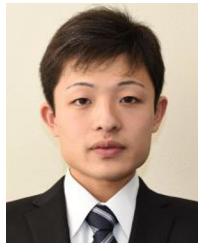

Yoshiaki Oto was born in Nagahama, Japan, in 1993. He received the B.Eng. and M.Eng. degrees in electrical and electronic engineering in 2015 and 2017, respectively, from Shizuoka University, Hamamatsu, Japan, where he is working toward the Ph.D. degree in engineering with the Department of Environment and Energy Systems, Graduate School of Science and Technology.

His research interests include motor drive technology with a dual-inverter system feeding an open-end-winding motor for hybrid vehicles.

Mr. Oto is a student member of the Institute of Electrical Engineers of Japan.

Toshihiko Noguchi (SM'02) was born in Kuwana, Japan, in 1959. He received the B.Eng. degree in electrical engineering from the Nagoya Institute of Technology, Nagoya, Japan, in 1982, and the M.Eng. and D.Eng. degrees in electrical and electronics systems engineering from the Nagaoka University of Technology, Nagaoka, Japan, in 1986 and 1996, respectively.

In 1982, he joined Toshiba Corporation, Tokyo, Japan. He was a Lecturer with the Gifu National College of Technology, Gifu, Japan, from 1991 to 1993. He was an Assistant Professor and an Associate Professor with the Department of Electrical, Electronics and Information Engineering, Nagaoka University of Technology, from 1994 to 1995 and from 1995 to 2009, respectively. Since 2009, he has been a Professor with the Department of Electrical and Electronics Engineering, Faculty of Engineering and Graduate School of Engineering, Shizuoka University, Hamamatsu, Japan. His research interests include new circuit topologies of static power converters and motor drives including electric machine hardware.

Dr. Noguchi is a member of the Institute of Energy Economics, Japan.

Takanari Sasaya received the B.E. and M.E. degrees in electrical and electronic engineering from Shizuoka University, Hamamatsu, Japan, in 1985 and 1987, respectively.

Since 1987, he has been with Denso Corporation, Nisshin, Japan, working on the research and development of gate drive circuits for power devices and power conversion systems for vehicular applications.

Mr. Sasaya is a member of the Institute of Electrical Engineers of Japan, the Society of Automotive Engineers of Japan, and the Japan Institute of Electronics Packaging.

Takahiro Yamada was born in Shizuoka, Japan. He received the master's degree in information engineering from Nagoya University, Nagoya, Japan, in 1996.

Since 1996, he has been with Denso Corporation, Nisshin, Japan, where he is involved in research and development of power electronics for automotive systems. His research interests include high-efficiency power conversion system and motor control.

Mr. Yamada is a member of the Institute of Electrical Engineers of Japan.

Ryoya Kazaoka was born in Nagoya, Japan. He received the master's degree in electrical engineering from Kyoto University, Kyoto, Japan, in 2013.

Since 2013, he has been with Denso Corporation, Nisshin, Japan, where he is involved in research and development of power electronics for automotive systems. His research interest include high-efficiency motor drives with SiC inverter systems.

Mr. Kazaoka is a member of the Institute of Electrical Engineers of Japan.