Fault Tolerant Operation of Motor Drive Fed by Dual Inverter Focusing on DC-Bus Battery Failure

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Abstract— A fault tolerant operation of the DC-bus battery in the dual inverter motor drive feeding an open-end winding motor is described in this paper. The dual inverter motor drive studied in this paper has a battery and a capacitor in parallel across the DC-bus of each inverter, and it is assumed that the battery across the DC-bus of one of the inverters is separated. The dual inverter motor drive has the redundancy of the switching state, which means that the particular voltage vectors can be generated with the several redundant states. In the fault tolerant operation, the failed inverter is operated with the capacitor instead of the failed battery, and the capacitor voltage is controlled at constant value by using the redundant switching state with a space vector modulation (SVM). In particular, the capacitor voltage of the failed inverter is required to be regulated at a half of the battery voltage of the normal condition inverter, in order to utilize the redundancy of the switching state. On the other hand, in the normal condition, the battery voltages of both inverters are same to expand the operation region of the dual inverter system, because the system can generate the voltage vector to the motor by adding the output voltages of two inverters. Therefore, it is necessary to discharge the capacitor voltage smoothly up to a half of the battery voltage of the normal condition inverter, immediately after the failed battery is separated. In this paper, the switching over techniques from the normal condition to the fault tolerant operation of the DC-bus battery with the SVM in the dual inverter motor drive are proposed. The proposed techniques are examined through several computer simulations and experimental tests.

Keywords—fault tolerant operation, space vector modulation, dual inverter motor drive, open-end winding motor, capacitor voltage control

I. Introduction

Recently, a mileage improvement and autopilot technologies of hybrid and electric vehicles are focused on. However, the current system drives the permanent magnet (PM) motor with a 2-level inverter, whose DC-bus voltage is boosted with a bidirectional chopper. The improvement of the efficiency in the current system is difficult because the large current flows into the voltage boost chopper, and the line to line voltage of the motor is a 2-level voltage waveform. And, it is also difficult to achieve a fault tolerant operation, because the current system cannot keep driving the motor if some failure is occurred in either the inverter or the chopper. Therefore, a dual inverter motor drive feeding an open-end winding motor with two inverters is focused on [1]-[10]. The dual inverter motor drive is expected to improve the efficiency of the system, because the system is not required any voltage boost converter and can generate a multilevel voltage waveforms across the motor windings. And, the dual inverter motor drive can achieve fault tolerant operations. So far, the fault tolerant operation of the switching device in the dual

inverter motor drive has been studied [11]-[13]. However, the fault tolerant operation, which assumes that the DC-bus battery of one of the inverters is failed, has not been studied. Therefore, the fault tolerant operations of the DC-bus battery are focused on and are discussed in this paper.

The dual inverter system studied in this paper has a battery and a capacitor in parallel across the DC-bus of each inverter. In this paper, it is assumed that the DC-bus battery of one of the inverters is in failure and is separated. In the fault tolerant operation of the DC-bus battery, the failed inverter is operated with the capacitor instead of the separated battery. The dual inverter system has a redundancy in the switching state, which means that the particular voltage vectors can be generated with the several redundant switching states. In this time, the capacitor voltage of the failed inverter must be controlled at constant value. However, the capacitor voltage is required to be regulated at a half of the battery of the normal condition inverter to utilize the capacitor charging/discharging modes among the redundant switching state. In order to select the switching state which charges/discharges the capacitor appropriately in the redundant switching states, a space vector modulation (SVM) is employed to operate the dual inverter motor drive in this paper. On the other hand, the DC-bus battery voltages of the dual inverter system are same value in the normal condition, in order to expand the operation region by increasing the amplitude of the output voltage which is generated by adding the output voltages of the two inverters. Therefore, it is necessary to discharge the capacitor voltage smoothly up to a half of the battery voltage of the normal condition inverter, immediately after some failure is detected in the battery and the failed battery is separated. In this paper, the SVM techniques to switch over the dual inverter system from the normal condition to the fault tolerant operation of the DC-bus battery are proposed. The proposed techniques are
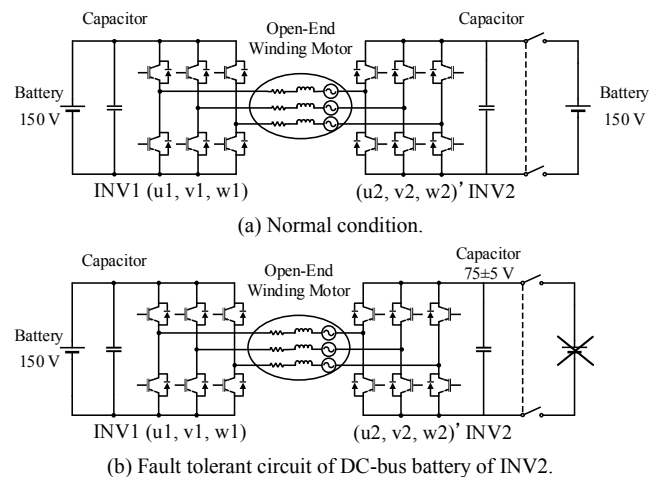

(a) Normal condition.

(b) Fault tolerant circuit of DC-bus battery of INV2.

Fig. 1. Circuit configurations of dual inverter motor drive.

examined through several computer simulations and experimental tests.

II. DUAL INVERTER MOTOR DRIVE

A. Circuit Configurations

The circuit configurations of the dual inverter motor drive studied in this paper are shown in Fig. 1, where the left-hand side and the right-hand side inverters are called INV1 and INV2, respectively. Each leg of both inverters is complementary operated, and the switching state of the dual inverter system is expressed as (u1, v1, w1) (u2, v2, w2)', where the switching state "1" means that the upper arm is turned on and "0" means the opposite. The both inverters have a battery and a capacitor across each DC-bus, whose voltages are same in the normal condition because the dual inverter system can expand the operation region by adding the output voltages of two inverters. The dual inverter system has the redundancy in the switching state, which can generate particular voltage vectors with the several redundant states. The redundancy can achieve the fault tolerant operation of the DC-bus battery.

B. Fault Tolerant Operation of DC-Bus Battery

In this paper, it is assumed that some failure is occurred in the DC-bus battery of the INV2 and the failed battery is separated with the relay across the DC-bus of the INV2. In the fault tolerant operation, the INV2 is operated with the capacitor instead of the failed battery, and the capacitor voltage is regulated at a half of the battery voltage of the INV1 as shown in Fig. 1 (b). The relationship between the switching states and the capacitor charging/discharging modes in the dual inverter motor drive enlarged from 0 to 60 degree is shown in Fig. 2. In case of the 1:1 DC-bus voltage ratio, either the charging or the discharging mode can be used in the redundant switching states. On the other hand, in case of the 1:0.5 DC-bus voltage ratio, both of the charging and the discharging modes can be used redundantly. Therefore, the 1:0.5 DC-bus voltage ratio is employed in this paper. However, the operation region of the dual inverter system of the 1:0.5 DC-bus voltage ratio is limited to $m < 0.5$, because the longest voltage vectors which configure the most outer hexagon do not have the redundancy, and the voltage vectors cannot be achieved the capacitor voltage control. That is why, the switching over techniques of the dual inverter motor drive from the normal condition to the fault tolerant operation of the DC-bus battery in case of $m < 0.5$ are discussed in this paper.

C. Space Vector Modulation

The dual inverter system has the redundancy in the switching state, which can generate the particular voltage with the several redundant states. Therefore, it is required to select the appropriate switching state among the redundant states, according to some requirements, in order to operate the dual inverter system. The SVM is employed to operate the dual inverter motor drive in this paper, because the SVM can select the switching state flexibly which charges/discharges the capacitor voltage appropriately among the several redundant states. Fig. 3 shows the principle of generating the command voltage vector v^* with the SVM, enlarged from 0 to 60 degree. An inverter can only discrete voltage vectors like V0 and V60 in Fig. 3. Therefore, it is necessarily to synthesize the available discrete voltage vectors at appropriate ratio, in order to generate the voltage vector with an arbitrary amplitude and an arbitrary phase in the SVM. In this time, the output time durations of each voltage vector in one SVM period are

(a) 1:1 DC-bus voltage ratio.   (b) 1:0.5 DC-bus voltage ratio.
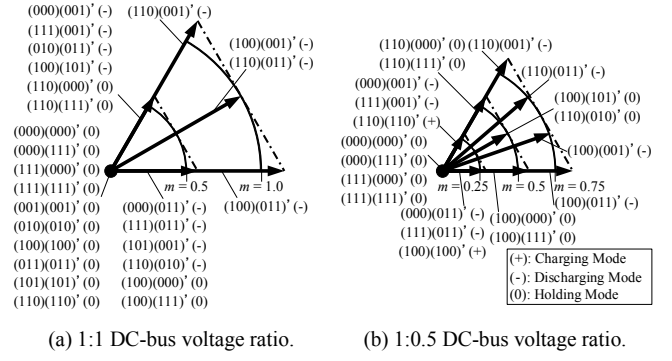
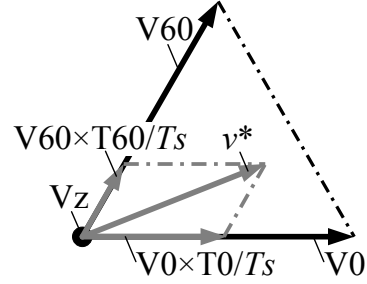Fig. 2. Redundancy of switching state in dual inverter motor drive enlarged from 0 to 60 degree.
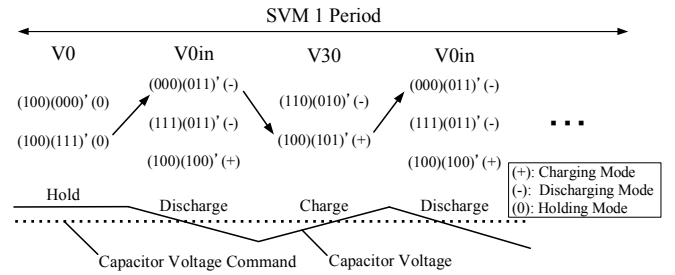

Fig. 3. Principle of SVM.

Fig. 4. Capacitor voltage control with SVM.

required to be calculated. The components of the voltage vectors V0 and V60 to synthesize the command voltage vector v^* are calculated as shown in Fig. 3, where Ts indicates the SVM control period, and T0 and T60 indicates the output time durations of the voltage vectors V0 and V60 during one SVM period, respectively. In the SVM, the three voltage vectors surrounding the region, where the command voltage vector v^* presents, are utilized to synthesize the command voltage vector. In case of Fig. 3, for example, the three voltage vectors V0, V60, and Vz are used for the SVM.

D. Capacitor Voltage Control

In the fault tolerant operation of the DC-bus battery, it is necessarily both to control the capacitor voltage of the failed inverter constantly and to generate the multilevel voltage waveforms across the motor windings, simultaneously. The capacitor voltage control is achieved with the redundancy of the switching state of the dual inverter motor drive with the 1:0.5 DC-bus voltage ratio. In this time, the SVM is required to select the appropriate switching state which charges/discharges the capacitor appropriately among the several redundant states. As shown in Fig. 4, when the voltage vector V0in is generated, the capacitor charging mode is selected if the capacitor voltage is lower than the command value, for example. In this way, the simultaneous control of the capacitor voltage and the multilevel voltage waveform generation can be achieved. However, the capacitor

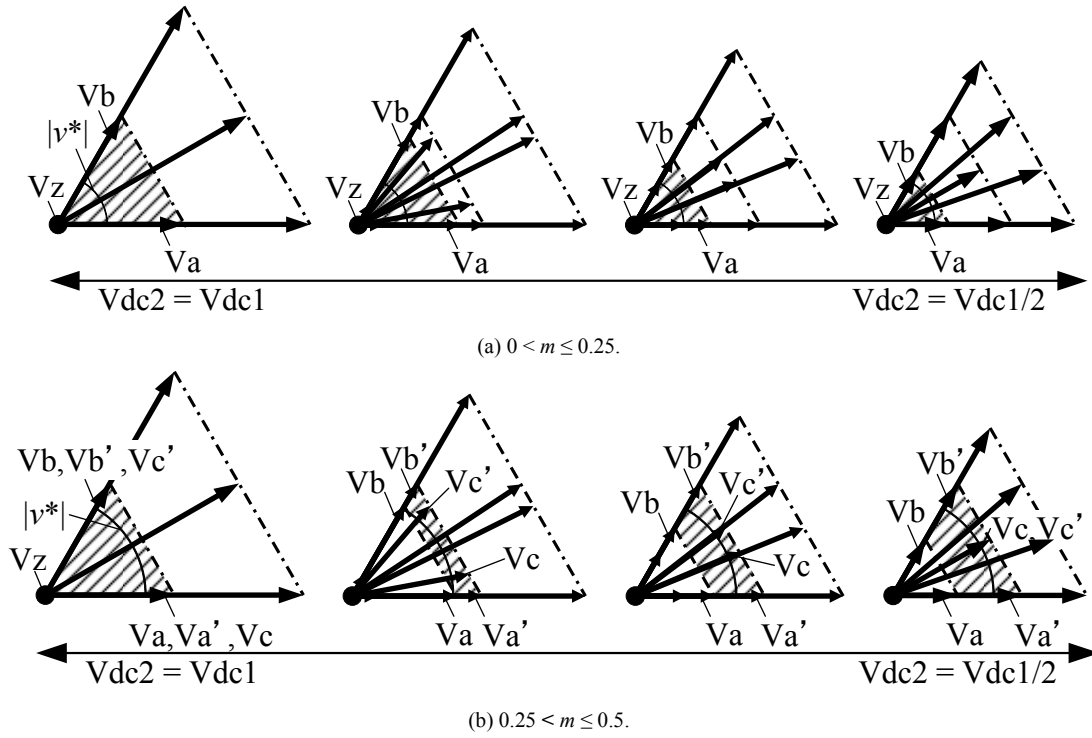(a) $0 < m \le 0.25$.

(b) $0.25 < m \le 0.5$.

Fig. 5. Proposed switching over technique for fault tolerant operation of DC-bus battery.

charging/discharging mode of each switching state may be changed, depended on the instantaneous motor power factor [14]. Therefore, the selection of the appropriate switching state among the redundant state must be implemented, considering the instantaneous motor power factor.

III. PROPOSED SWITCHING OVER TECHNIQUE FOR FAULT TOLERANT OPERATION

The dual inverter system in the normal condition is operated with the 1:1 DC-bus voltage ratio, in order to expand the operation region of the system. On the other hand, the fault tolerant operation of the DC-bus battery is required to regulate the capacitor voltage of the failed inverter at a half of the battery voltage of the normal condition inverter. Therefore, the SVM techniques to discharge the capacitor voltage of the failed inverter smoothly up to a half of the battery voltage of the normal condition inverter, immediately after the failed battery is separated, while generating the command voltage vector across the motor windings at the same time, are proposed. The proposed SVM techniques to switch over the dual inverter motor drive from the normal condition to the fault tolerant operation assume two cases of the modulation index, which is $0 < m \le 0.25$ and $0.25 < m \le 0.5$ as shown in Fig. 5 (a) and (b), respectively.

The dual inverter motor drive has particular switching states to generate the voltage vectors Va and Vb in Fig. 5 (a), which utilize only the capacitor voltage of the INV2 to generate the voltage vectors, and simultaneously can discharge the capacitor voltage. In case of $0 < m \le 0.25$, therefore, the proposed SVM technique is implemented with the voltage vectors Va, Vb, and the zero voltage vector Vz, which has the zero amplitude and keeps the capacitor voltage by disconnecting the capacitor from the dual inverter circuit. However, the switching state to generate the voltage vector Va or Vb must be selected to discharge the capacitor of the failed inverter and to utilize only the capacitor voltage to generate the voltage vector among the redundant states with the SVM. In other words, the selected switching state can achieve both

to discharge the capacitor of the failed inverter and to generate the voltage vector Va or Vb with the amplitude which is variable depending on only the capacitor voltage. In this way, the SVM can switch over the dual inverter system from the normal condition to the fault tolerant operation of the DC-bus battery, while outputting the command voltage vector to the motor, according to the capacitor voltage of the INV2 discharged up to a half of the battery voltage of the INV1 as shown in Fig. 5 (a).

On the other hand, in case of $0.25 < m \le 0.5$, the voltage vectors Va', Vb', Vc, and Vc' are used for the SVM in addition to the voltage vectors Va and Vb whose amplitudes depend on only the capacitor voltage of the INV2. The voltage vectors Va' and Vb' are generated with only the voltage of the INV1, that is, the amplitudes of the Va' and Vb' do not depend on the capacitor voltage of the INV2. The amplitudes of the voltage vectors Vc and Vc' are variable depended on the battery voltage of the INV1 and the capacitor voltage of the INV2 as shown in Fig. 5 (b), because the voltage vectors are generated by adding the output voltage vectors of the INV1 and the INV2. At first, the SVM to switch over the dual inverter system to the fault tolerant operation in case of $0.25 < m \le 0.5$ is performed in the same way as $0 < m \le 0.25$, until the straight line between the voltage vectors Va and Vb inscribes the circle locus of the rotating command voltage vector. Subsequently, the SVM is performed on the basis of the three triangle regions. Every triangle region is surrounded with the three voltage vectors, that is, (Va, Va', Vc/Vc'), (Va', Vb', Vc/Vc'), and (Vb, Vb', Vc/Vc'). In this time, "Vc/Vc'" means that either the voltage vector Vc or Vc' is selected appropriately, considering the instantaneous motor power factor, and is used for the SVM because either the voltage vector Vc or Vc' is the capacitor charging mode. In this way, the proposed SVM techniques achieve to switch over the dual inverter system smoothly from the normal condition to the fault tolerant operation of the DC-bus battery in case of $m < 0.5$, while generating the command voltage vector to the motor at the same time.

IV. Computer Simulations

A. Computer Simulation Conditions

Computer simulations have been conducted to examine the proposed SVM techniques to switch over the dual inverter system from the normal condition to the fault tolerant operation smoothly. The control block diagram is indicated in Fig. 6, where a surface permanent magnet (SPM) motor with an open-end windings is controlled with a field-oriented control (vector control) algorithm, so has a speed control loop and a current control loop in the controller. The instantaneous motor power factor is calculated from the phase difference between the command voltage vector and the motor line current vector on the synchronously rotating (d-q) reference frame, which is utilized to select the appropriate switching state among the redundant states, as well as the feedback value of the capacitor voltage of the INV2. A relay to simulate the separation of the battery of the INV2 is inserted between the battery and the capacitor across the DC-bus of the INV2. The dual inverter system in the normal condition starts to transfer the fault tolerant operation with the proposed SVM techniques after the separation of the battery of the INV2 is detected with the fault signal in Fig. 6. In other words, the capacitor voltage of the INV2 is discharged from 150 V to approximately 75 V with the proposed SVM techniques after the DC-bus battery separation is occurred in the INV2. Then, the capacitor voltage is controlled within 75±5 V with the redundant switching states in the fault tolerant operation. However, the simulations are conducted under the ideal condition, that is, there is no dead time.
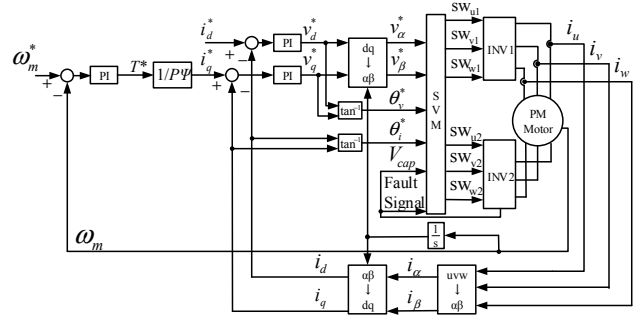

Fig. 6. Control block diagram.

TABLE I. COMPUTER SIMULATION CONDITIONS

Switching frequency		10 kHz
Battery voltages in normal condition		150 V
Capacitor voltage command in fault tolerant operation		75±5 V
Capacitance of DC-bus capacitor		1330 μF
Dead time		0 μs
Motor parameters	Number of poles	4
	Number of flux linkage	0.174 Wb
	Moment of inertia	0.00137 kgm^2
	Damping coefficient	0.01 N/rad/s
	Phase resistance	1.1 Ω
	Phase inductance	5 mH

(a) m = 0.2 (600 r/min).
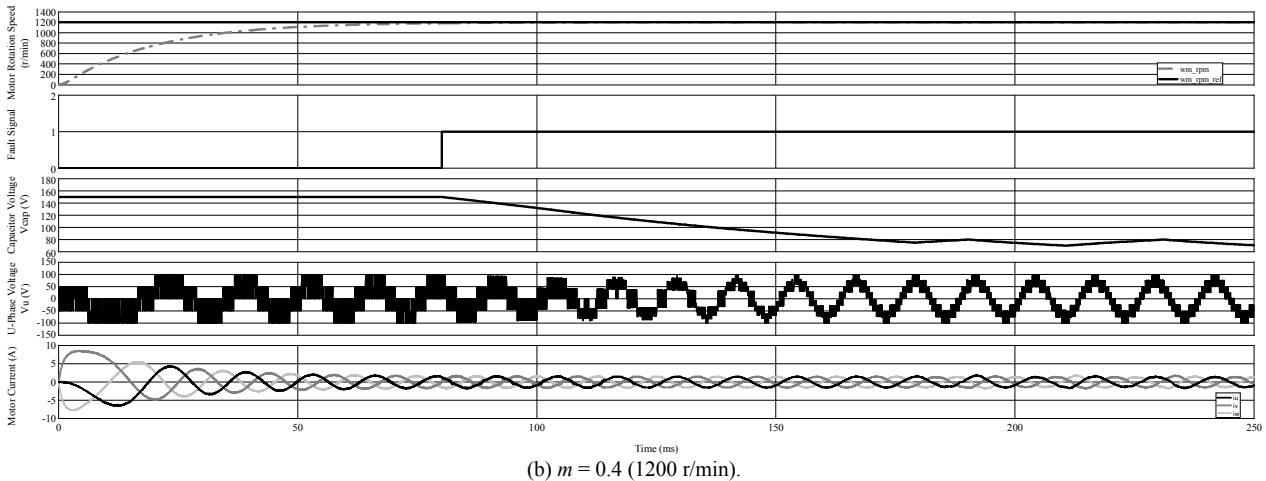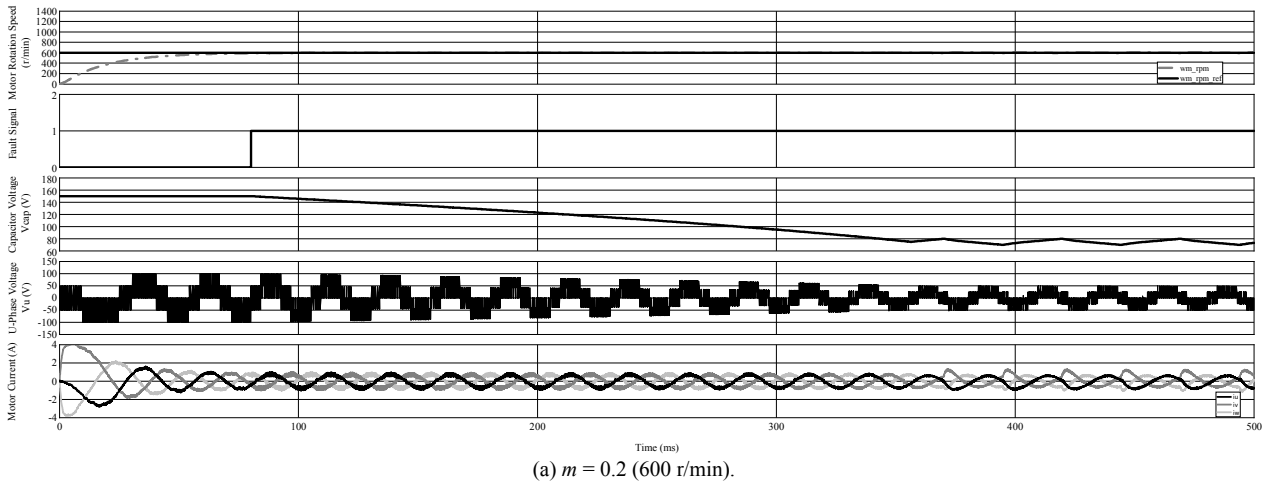

(b) m = 0.4 (1200 r/min).

Fig. 7. Computer simulation results.

B. Computer Simulation Results

The simulation results in case of the modulation index m = 0.2 and m = 0.4 are shown in Fig. 7 (a) and (b), respectively. In the figures, the motor rotating speed, the fault signal, the capacitor voltage, the U-phase voltage, and the motor line currents are indicated. In the dual inverter motor drive in the normal condition where both inverters are operated with the battery with 150 V, the 5-level voltage waveforms are generated between the motor winding terminals of each phase at m = 0.2 and m = 0.4. On the other hand, the dual inverter motor drive in the fault tolerant operation, in case of $0 < m \leq$ 0.25, can generate the 5-level voltage waveforms with a half amplitude of the normal condition as shown in Fig. 7 (a), that is, with a closer amplitude to the command voltage vector than the normal condition. Therefore, it is expected to reduce the harmonic component rate of the output voltage waveforms in the fault tolerant operation, which results in the improvement of the total harmonic distortion (THD). And, the dual inverter motor drive in the fault tolerant operation, in case of $0.25 < m \leq 0.5$, can generate the 9-level voltage waveforms across the motor windings as shown in Fig. 7 (b), which also results in the improvement of the THD. In addition, at the both cases, the dual inverter motor drive achieves to transient from the normal condition to the fault tolerant operation smoothly with the proposed SVM techniques, while generating the constant command voltage vector to the motor, as can be seen from the figures.

V. EXPERIMENAL TESTS

A. Experimental Setup

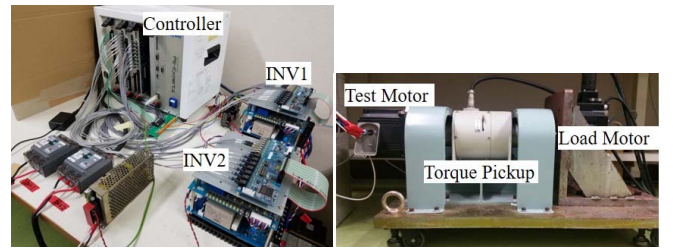The experimental setup of the dual inverter motor drive has been conducted to examine the proposed SVM techniques

Fig. 8. Experimental setup of dual inverter motor drive.

TABLE II.   PARAMETERS OF TEST MOTOR

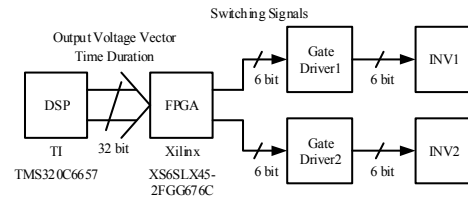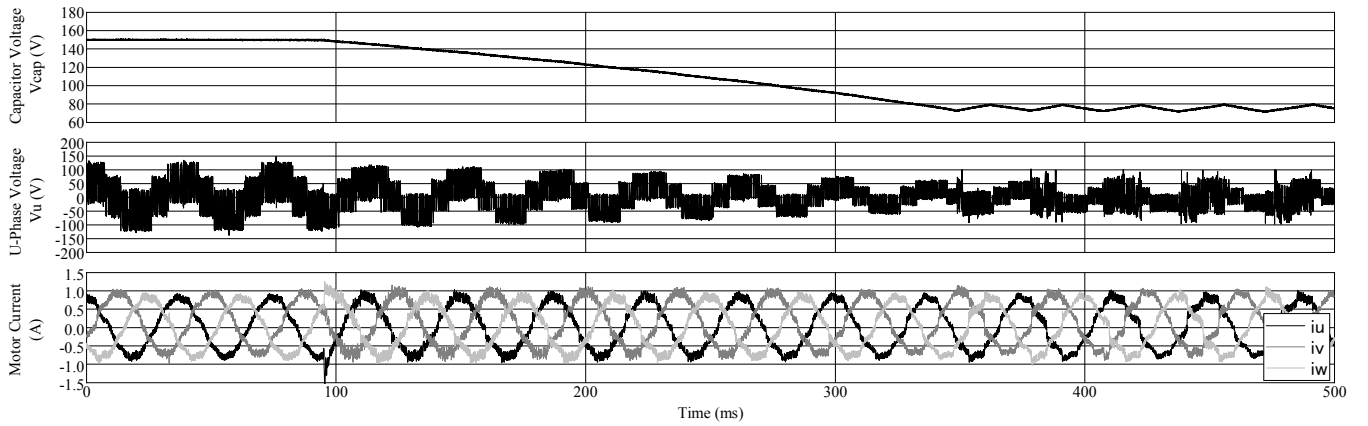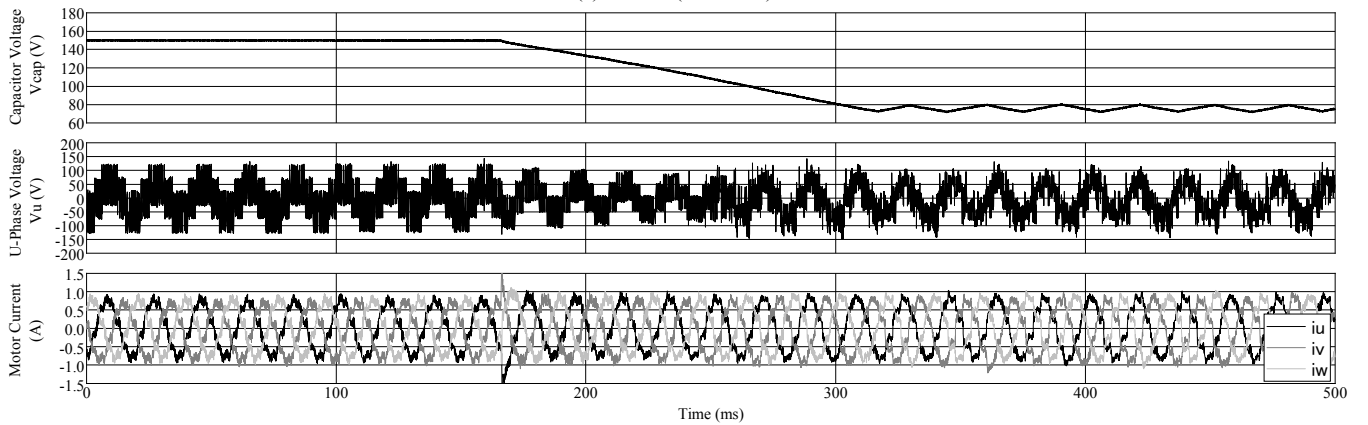| Number of poles	4
Rated power	1000 W
Rated speed	2000 r/min
Rated torque	4.78 Nm
Rated current	3.7 A
Armature resistance	1.1 Ω
Number of flux linkage	0.174 Wb
d-axis inductance	11.0 mH
q-axis inductance	25.0 mH

Fig. 9. Block diagram of controller.

(a) m = 0.2 (400 r/min).

(b) m = 0.4 (800 r/min).

Fig. 10. Experimental test results.

to switch over the system from the normal condition to the fault tolerant operation as shown in Fig. 8, where the 1-kW open-end winding interior permanent magnet (IPM) motor is controlled with a vector control algorithm and a maximum torque per ampere (MTPA) control method by the two 5-kVA inverters. The control block diagram and the experimental conditions are similar to the computer simulations in Fig. 6 and Table I, but the motor rotating speed is regulated by the load servo motor directly connected to the open-end winding test motor, and the dead time is set to 4 μs. The SVM to control the dual inverter motor drive is implemented in the digital signal processor (DSP) and the field programmable gate array (FPGA) as shown in Fig. 9. The detections of the region where the command voltage vector presents, the selection of the voltage vectors which are utilized for the SVM, and the calculations of the time durations are implemented in the DSP. And, the FPGA outputs the switching signals to the gate drivers of both inverters with the high resolution of 100 MHz according to the calculation results of the DSP .

B. Experimental Test Results

The experimental test results of the modulation index $m = 0.2$ and $m = 0.4$ are shown in Fig. 10 (a) and (b), respectively. In the figures, the capacitor voltage, the U-phase voltage, and the motor line current are indicated. The similar operation characteristics to the computer simulation results have been verified in the experimental test results. However, the voltage waveforms of the dual inverter motor drive in the fault tolerant operation have a lot of error voltage pulses. The error voltages are generated during the dead time of the transient between the particular switching states, where the switching devices in the same phase of both inverters are synchronously turned on/off, and the several switching devices in one inverter are synchronously turned on/off. Therefore, the SVM techniques to reduce the error voltages are introduced [15][16]. The SVM implemented in this paper employs the introduced techniques. All in all, the proposed SVM techniques to switch over the dual inverter drive from the normal condition to the fault tolerant operation smoothly have been verified to work well.

VI. CONCLUSION

In this paper, the fault tolerant operation of the DC-bus battery in case of $m < 0.5$ in the dual inverter motor drive is discussed. In the fault tolerant operation, the failed inverter is operated with the capacitor instead of the failed battery. Therefore, it is required to control the capacitor voltage at constant value, in particular, the redundancy of the switching state can be utilized by regulating the capacitor voltage at a half of the battery voltage of the normal condition inverter. Therefore, it is necessary to discharge the capacitor voltage up to a half of the battery voltage of the normal condition inverter, immediately after some failure is detected in the battery and the failed battery is separated. In this paper, the SVM techniques to switch over the dual inverter motor drive from the normal condition to the fault tolerant operation smoothly are proposed. And, the validity of the proposed SVM techniques have been verified through the computer simulations and the experimental tests. The consideration of the fault tolerant operation in case of $m > 0.5$ in the dual inverter motor drive is one of the future works of the authors.

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