IEEJ Journal of Industry Applications
Vol.8 No.6 pp.953–959 DOI: 10.1541/ieejjia.8.953

Paper

Fault-Tolerant Function of DC-Bus Power Source in A Dual Inverter Drive System and Its Operation Characteristics

Yoshiaki Oto[*a)] Student Member, Toshihiko Noguchi[*] Member

(Manuscript received March 4, 2019, revised June 13, 2019)

The dual inverter drive system feeding an open-end winding permanent magnet (PM) motor has been studied for developing autopilot technologies of hybrid vehicles. Autopilot systems require fault-tolerant functions, which enable it to continue to drive the motor even if some failure occurs in the motor drive system. The fault-tolerant function of a dual inverter drive system, which assumes that the DC-bus battery power source of the dual inverter drive system has failed, is discussed in this paper. In the dual inverter drive system that is considered, both the inverters have a capacitor in parallel with a battery across each DC-bus. The capacitor drives the motor continuously even if the DC-bus battery has failed. The inverter, in which the DC-bus battery has failed, is operated with the capacitor instead of the failed battery. It is required to both control the capacitor voltage at a constant value and simultaneously generate multilevel voltage waveforms across the motor windings with the space vector modulation (SVM). In this paper, the fault-tolerant function of the DC-bus battery in a dual inverter drive system is proposed, and its operation characteristics are examined through several experiments and compared with those of a normal system.

Keywords: fault-tolerant function, dual inverter drive system, open-end winding motor, capacitor voltage control, space vector modulation

1. Introduction

In recent years, autopilot technologies and mileage improvement techniques of hybrid vehicles are focused on. Many of the current hybrid vehicles drive a high-voltage permanent magnet (PM) motor with the combination of a bidirectional chopper and a two-level inverter. Therefore, it is difficult to improve the efficiency of the current system due to the bidirectional chopper where large current flow for the voltage boost. The current system also cannot continue to drive the motor if either the chopper or the inverter has failed. And, the line-to-line voltage of the motor is a three-level waveform, which may cause deterioration of the total harmonic distortion (THD), conduction noise, and radiation noise. Therefore, the dual inverter drive system, where two 2-level inverters feed an open-end winding PM motor, has been focused on [(1)–(5)]. The dual inverter drive system is expected to improve the efficiency of the system, because the system can generate the multilevel voltage waveforms across the motor windings by adding the voltages of the two inverters, and it is not required any voltage boosting chopper. In particular, the dual inverter drive system, where the DC-bus battery of one of the inverters is replaced with a capacitor, has been studied [(6)–(16)]. The dual inverter drive system can achieve several fault-tolerant functions and also can output multilevel voltage waveforms across the motor windings. The fault-tolerant function means that the system can continue to drive the motor even if some failure occurs in the system. So far, the fault-tolerant techniques of inverter switching device have been studied, however, the fault-tolerant technique of the DC-bus battery has not been studied in dual inverter drive system [(17)–(19)].

The dual inverter drive system where both the inverters have a battery and a capacitor in parallel across each DC-bus is studied, and its fault-tolerant function of the DC-bus battery is proposed in this paper. The proposed fault-tolerant function can continue to drive the motor even if the DC-bus battery of the dual inverter drive system has failed, because the failure-side inverter is operated with the capacitor instead of the failed battery. In the case, it is necessary to control the capacitor voltage constantly, generating the multilevel voltage waveforms across the motor windings by the phase difference of the fundamental voltage components between the two inverters [(10)(11)]. In the proposed method, the space vector modulation (SVM) is employed and the redundancy of the switching states of the dual inverter drive system is focused on. In this paper, the dual inverter drive system which has been studied by authors is adopted for the fault-tolerant function of the DC-bus battery [(20)], and the operation characteristics are examined through additional experimental tests to compare the operation characteristics of the normal-condition and the failure-condition.

2. Configuration of Dual Inverter Drive System

Figure 1 shows a circuit diagram of the conventional motor

a) Correspondence to: Yoshiaki Oto. E-mail: ohto.yoshiaki.15@shizuoka.ac.jp
* Department of Electrical and Electronics Engineering, Faculty of Engineering, Shizuoka University
3-5-1, Johoku, Naka-ku, Hamamatsu, Shizuoka 432-8561, Japan

This work was supported by the New Energy and Industrial Technology Development Organization (NEDO) Grant-in-Aid for Scientific Research from the National Government and Ministry of Economy, Trade and Industry, Japan.

© 2019 The Institute of Electrical Engineers of Japan.

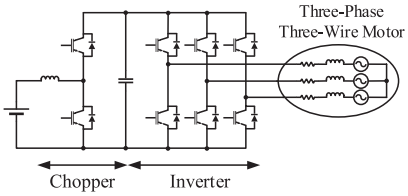


Fig. 1. Conventional motor drive system of hybrid vehicles with single inverter drive system

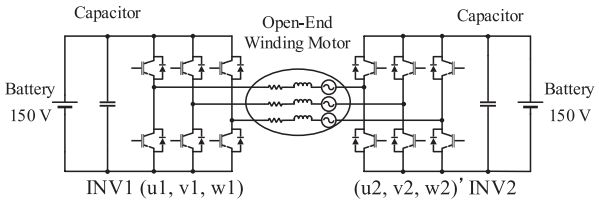


Fig. 2. Studied motor drive system of hybrid vehicles with dual inverter drive system

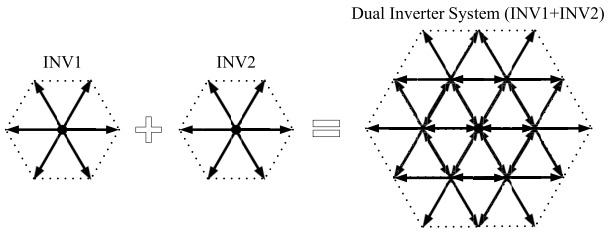


Fig. 3. Principle of voltage vector generation of dual inverter drive system

drive system of hybrid vehicles which consists of a bidirectional chopper, a single two-level inverter, and a three-phase PM motor with a neutral-point inside of the motor. Figure 2 shows the dual inverter drive system studied in this paper, where the left-hand side and right-hand side inverters are called INV1 and INV2, respectively. Both the inverters have a capacitor in parallel with a battery across each DC-bus. Each leg of both the inverters is complementary operated, and the combination of the switching states is expressed as (u1, v1, w1) (u2, v2, w2)', where the switching state "1" means that the upper arm is turned on and the "0" means the opposite. The studied dual inverter drive system has the advantages of generating the multilevel voltage waveforms and utilizing the redundancy of the switching states. And also, the studied system does not require any voltage boost power converter such as the bidirectional chopper, however, the inverter counts and the DC-bus power source counts are increased, compared with the conventional single inverter motor drive system.

The dual inverter drive system can output the voltage vector by adding the voltage vectors generated with the INV1 and the INV2 as shown in Fig. 3, therefore, the system can generate the multilevel voltage waveforms across the motor windings. The multilevel voltage waveform generation can reduce the dv/dt and the harmonic component rate of the output voltage waveforms, which results in the improvement of the THD. It is expected to reduce the copper and the iron losses as a result of the improvement of the THD of the output multilevel voltage waveforms and is expected to reduce the conduction and the radiation noises as a result of the

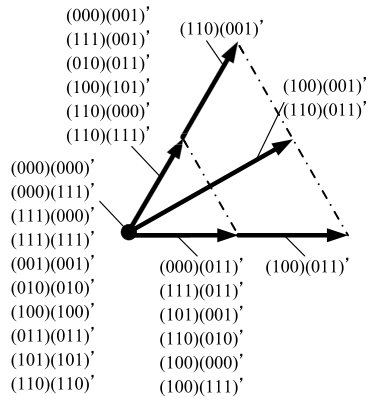
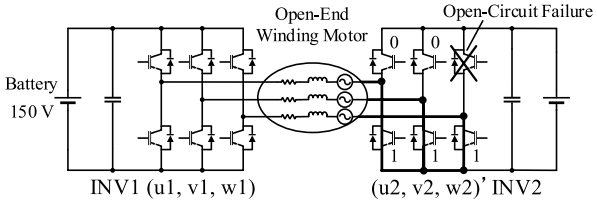
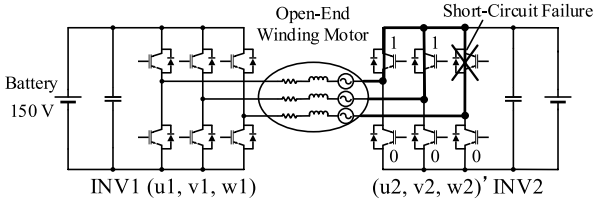


Fig. 4. Redundant switching states of normal-condition dual inverter drive system enlarged from 0 to 60 degree



(a) Open-circuit failure of switching device of upper arm in W-phase of INV2.



(b) Short-circuit failure of switching device of upper arm in W-phase of INV2.

Fig. 5. Conventional fault-tolerant functions of one of inverter switching devices

reduction of the dv/dt. The dual inverter drive system also has the redundancy in the switching states, which means that particular voltage vectors can be generated to the motor with the several different redundant switching states as shown in Fig. 4. The studied dual inverter drive system can achieve the proposed fault-tolerant functions with the redundancy of the switching states with the SVM.

The conventional fault-tolerant function of one of the inverter switching devices has been studied [17]–[19]. The failure-side inverter where one of the inverter switching devices has failed makes the neutral-point of the motor by shorting the normal-condition arms as shown in Fig. 5, that is, the failed inverter keeps the switching state either (000) or (111). The fault-tolerant functions of the switching device of the upper arm in the U-phase of the INV2 is in the open-circuit failure and the short-circuit failure are shown in Figs. 5(a) and (b), respectively. The conventional fault-tolerant function makes it possible that the studied dual inverter drive system can continue to operate the motor as a single inverter motor drive system, even if one of the inverter switching devices has failed. The conventional function also may achieve the fault tolerance of the DC-bus battery as the single inverter drive system by making the short circuit with the inverter whose DC-bus battery has failed. On the other hand, the proposed fault-tolerant function is operated as the dual inverter system by utilizing the capacitor voltage control with the space vector

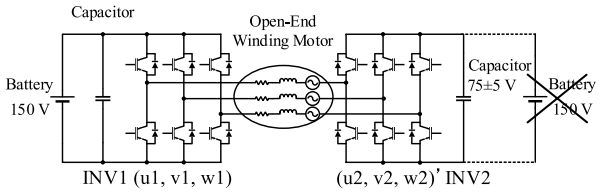


Fig. 6. Proposed fault-tolerant function of DC-bus battery of INV2

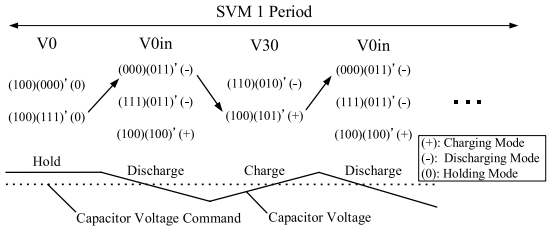
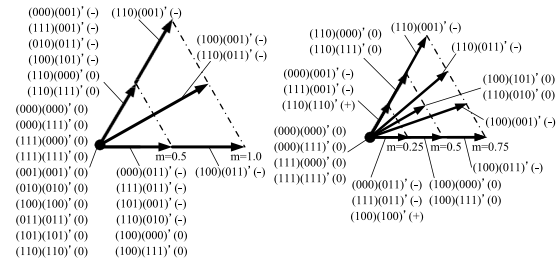


Fig. 7. Simultaneous control of multilevel voltage waveform generation and capacitor voltage across DC-bus of failure-side inverter with SVM



(a) Dual inverter with 1:1 DC-bus voltage ratio.

(b) Dual inverter with 1:0.5 DC-bus voltage ratio.

Fig. 8. Relationship between output voltage vectors from 0 to 60 degree and capacitor charging/discharging modes in steady state

modulation. Therefore, the proposed function is expected to improve the THD of the output voltage waveforms, that is, to reduce harmonic losses because the proposed function can generate the multilevel voltage waveforms across the motor windings.

3. Proposed Fault-Tolerant Function of DC-Bus Battery with SVM

The fault-tolerant function of DC-bus battery is proposed in this paper, which is achieved with the capacitor voltage control across the DC-bus of the failed inverter. Figure 6 is assumed that the proposed fault-tolerant function of the DC-bus battery source of INV2. The fault detection of the DC-bus battery can be achieved with the current and voltage sensors in the system. The over current of the battery can be detected with the current sensor of the DC-bus. And, the separation of the battery can be detected with the voltage sensors which is in the battery management system of the battery. Then, the separation of the DC-bus battery can be achieved with the electromagnetic contactor of the DC-bus. In the case, the failure-side inverter is operated with the capacitor, which is connected in parallel to the battery across the DC-bus. In the proposed fault-tolerant function, it is necessary both to generate the multilevel voltage waveforms to the motor and simultaneously to control the capacitor voltage across the DC-bus of the failure-side inverter constantly. As described before, the dual inverter drive system has the redundancy in the switching states, which makes it possible to generate particular voltage vectors with the several different redundant states. The capacitor charging or discharging modes of the each switching state can be calculated by the directions of the motor phase currents. Both of the capacitor voltage control of the failed inverter and the multilevel voltage waveform generation can be achieved with the SVM by selecting the appropriate switching state in the redundant states, which charges or discharges the capacitor voltage appropriately as shown in Fig. 7. The SVM is employed to operate the proposed fault-tolerant function, because the switching sequence can be designed flexibly in the SVM.

The 1:0.5 voltage ratio is employed to utilize the redundancy of the switching states in the proposed fault-tolerant function, which means that the capacitor voltage across the DC-bus of the failed inverter is regulated at a half of the battery voltage of the normal-condition inverter. The relationship between the output voltage vectors from 0 to 60 degree and the capacitor charging/discharging modes in the steady-state is shown in Fig. 8. As shown in the figure, both the capacitor charging and discharging modes can be used redundantly in particular redundant switching state in case of the 1:0.5 DC-bus voltage ratio, on the other hand either the capacitor charging or discharging mode can be used in particular redundant states in case of the 1:1 DC-bus voltage ratio. That is why the 1:0.5 DC-bus voltage ratio is employed, and the capacitor voltage of the failed inverter should be controlled at a half of the DC-bus battery voltage of the normal-condition inverter in the proposed fault-tolerant function.

The modulation-index m is also indicated in Fig. 8. The dual inverter system can generate the voltage vectors by adding the voltages of the two inverters. However, the proposed failure-condition system cannot generate the voltage vectors in $m > 0.5$, because the system is required to achieve both the capacitor voltage control and the voltage waveform generation to the motor at the same time. Therefore, the maximum motor rotating speed of the proposed failure-condition system is limited to a half of the normal-condition system. On the other hand, the proposed failure-condition system is expected to improve the THD of the output voltage waveforms because the system can generate the multilevel voltage waveforms across the motor windings. The proposed failure-condition system can generate the voltage vectors with a half amplitude of the normal-condition system in $m < 0.25$, that is, with the closer amplitude to the voltage reference than the normal-condition. Therefore, the harmonic content rate of the output voltage waveforms and the harmonic losses in the failure-condition system are reduced in $m < 0.25$, which result in the improvement of the THD of the output voltage waveforms. On the other hand, the harmonic losses and the THD of the proposed failure-condition system is also expected to be improved in $0.25 \leq m < 0.5$, compared with the normal-condition system, because the proposed system can generate the 9-level voltage waveforms although the normal-condition system generates the 5-level voltage waveforms. That is why, the efficiency of the INV1 and the motor in the proposed system is expected to be improved.

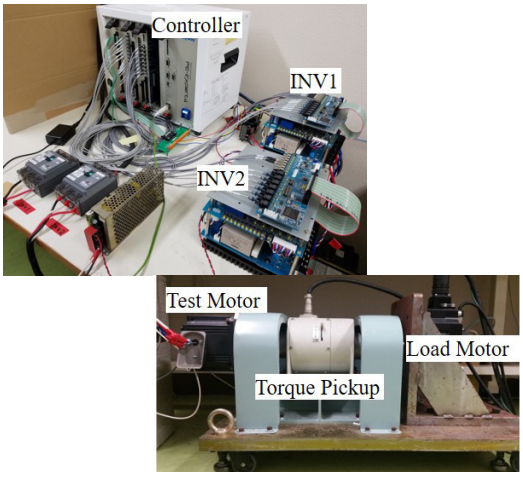


Fig. 9. Experimental setup of dual inverter drive system

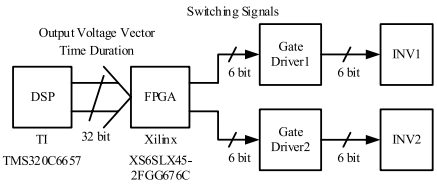


Fig. 10. Block diagram of controller

4. Experimental Setup and Test Results

4.1 Experimental Setup As shown in Fig. 9, the experimental setup of the dual inverter drive system has been conducted to examine the steady operation characteristics of the studied dual inverter drive system in the normal-condition and the failure-condition of the DC-bus battery. The SVM is implemented in the digital signal processor (DSP) and the field programmable gate array (FPGA) of the controller as shown in Fig. 10, where the DSP calculates the time durations of the output voltage vectors and communicates the results to the FPGA, and the FPGA outputs the switching signals to the gate drivers of the INV1 and the INV2 with the high resolution of 100 MHz. The open-end winding PM motor is controlled by a field-oriented control (vector control) algorithm with the maximum torque per ampere (MTPA) control method as shown in Fig. 11, and its speed is regulated constantly by a load servo motor directly connected to the test motor. The rated output power of the test motor is 1 kW which is fed by the two 5-kVA inverters, and other experimental test conditions are shown in Table 1.

As described before, the proposed fault-tolerant function achieves both to control the capacitor voltage across the DC-bus of failed-side inverter and to generate the multilevel voltage waveforms to the motor at the same time with the SVM. In this case, it is required to select the appropriate switching state among the redundant states considering the instantaneous motor power factor, because the capacitor charging/discharging modes of each switching state can be determined by the directions of the motor phase currents [20]. That is why, the phases of the commanded voltage vector and the motor current vector are calculated with the feedback value of the capacitor voltage, and are utilized to control the capacitor voltage constantly in the SVM as shown in Fig. 11.

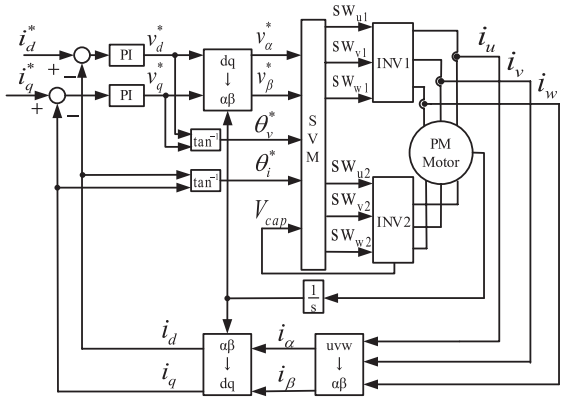


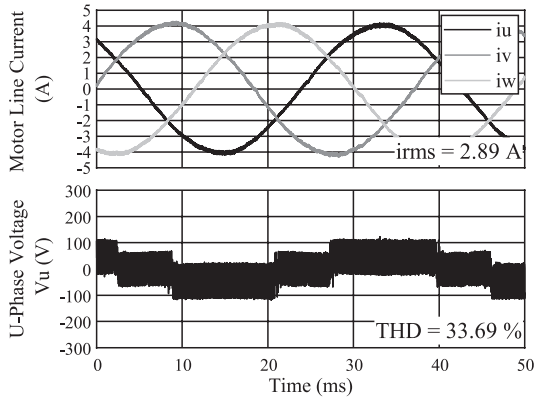
Fig. 11. Control block diagram

Table 1. Experimental test conditions

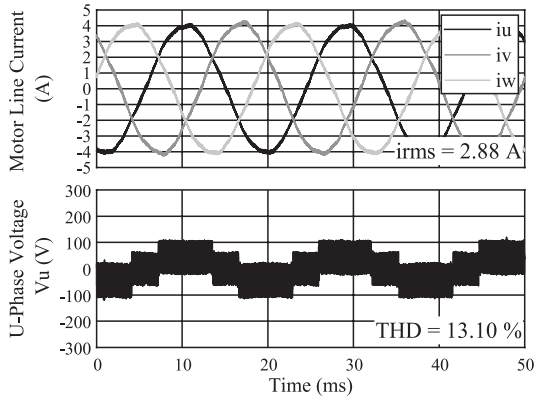
Switching frequency		10 kHz
Voltage of battery (INV1)		150 V
Voltage of battery (INV2)		150 V
Capacitor voltage command of failed inverter (INV2)		75 V
Capacitance of capacitor across DC-bus		1330 μF
Norm of current command		5 A
Motor speed		200, 400, 800, 1600 r/min
Dead time		4 μs
Motor parameters	Number of poles	8
	Rated power	1000 W
	Rated speed	2000 r/min
	Rated torque	4.78 Nm
	Rated current	3.7 A
	Armature resistance	1.1 Ω
	Number of flux linkage	0.174 Wb
	d-axis inductance	11.0 mH
	q-axis inductance	25.0 mH

4.2 Test Results of Dual Inverter Drive System in Normal-Condition The test results of the studied dual inverter drive system in the normal-condition are shown in Fig. 12. The figures show the three-phase motor currents and the voltages across the U-phase. On the condition of $m < 0.5$, the 5-level voltage waveforms are generated across the motor windings. In the case, the INV2 outputs the switching state (000) or (111) throughout the SVM, in other words, the INV2 makes the neutral-point of the motor. Therefore, it is difficult to measure the efficiency of the INV2 in $m < 0.5$. And also, the output voltage waveforms in Figs. 12(a) and (b) are similar to the voltage waveforms which is measured between the U-phase terminal and the neutral-point of the motor in a single inverter system. On the other hand, the 9-level voltage waveform is generated by adding the voltages of the INV1 and the INV2 in $m > 0.5$.

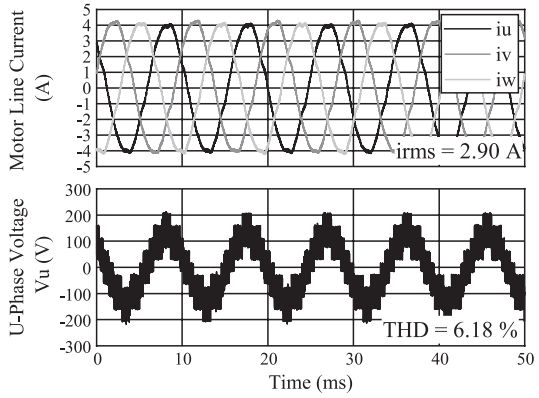
4.3 Test Results of Proposed Fault-Tolerant Function of DC-Bus Battery The experimental test results of the proposed fault-tolerant function are shown in Fig. 13 and Table 2, where the steady operation characteristics of the dual inverter drive system in the failure-condition of the DC-bus



(a) m = 0.2 (400 r/min).



(b) m = 0.4 (800 r/min).



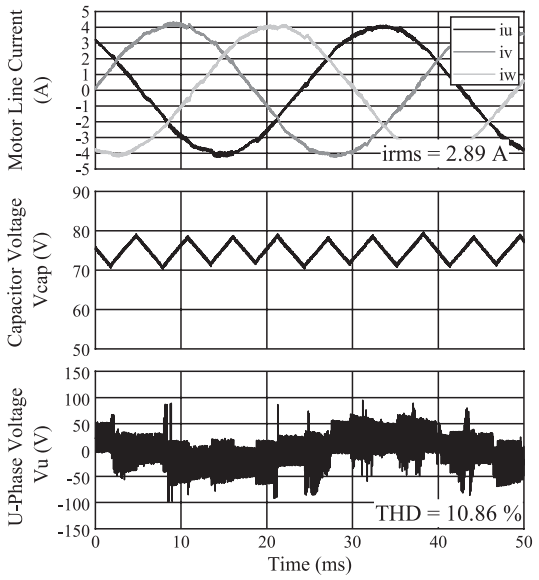
(c) m = 0.8 (1600 r/min).

Fig. 12. Test results of dual inverter drive system in normal-condition

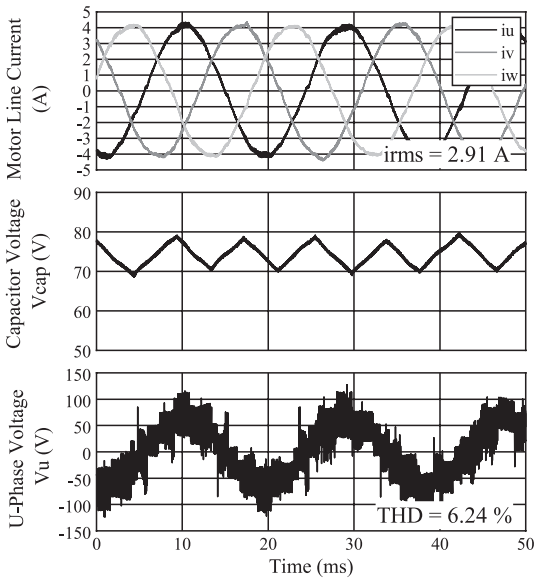
Table 2. Measured efficiency results

	Normal-condition			Failure-condition	
	m = 0.2	m = 0.4	m = 0.8	m = 0.2	m = 0.4
INV1	94.5 %	96.8 %	92.8 %	95.3 %	97.4 %
INV2			71.7 %		
Motor	66.2 %	71.7 %	73.3 %	66.5 %	71.8 %

battery of INV2 are examined. In the figures, the motor line current, the capacitor voltage, and the U-phase voltage are shown, which indicate that the SVM achieves both to control the capacitor voltage of the INV2 at a half of the battery voltage of INV1 and simultaneously to generate the multi-level voltage waveforms to the motor. The table shows the measured efficiency results of the INV1, the INV2, and the



(a) m = 0.2 (400 r/min).



(b) m = 0.4 (800 r/min).

Fig. 13. Test results of proposed fault-tolerant function of DC-bus battery of INV2

motor on the condition of each modulation-index. The efficiency measured results are calculated with the following equation. In the equation, η_{motor} is the motor efficiency, P_{INV1} and P_{INV2} are the output of the INV1 and INV2, ω_m is the motor rotating speed, and T is the motor torque.

$$\eta_{motor} = \frac{\omega_m T}{P_{INV1} + P_{INV2}}$$

However, P_{INV2} is only a conduction loss in the normal-condition in $m < 0.5$, which is a negative value, because the INV2 makes the neutral-point of the motor and there are no switching transitions. On the other hand, P_{INV2} is the sum of a conduction loss and a switching loss in the failure-condition in $m < 0.5$, which is also a negative value, because the INV2 is operated with the capacitor and the capacitor utilizes only a reactive power. That is why, the efficiency of the INV2 cannot be obtained at m = 0.2 and m = 0.4 in the normal-condition and in the failure-condition. In the experimental

tests, however, it is not achieved to switch over the dual inverter drive system from the normal-condition to the failure-condition transiently.

The proposed fault-tolerant function can generate the voltage vectors with a half amplitude of the normal-condition system in $m < 0.25$, that is, with the closer amplitude to the voltage reference than the normal-condition system as shown in Fig. 8, which result in the reduction of the harmonic content rate of the output voltage waveforms. That is why, the measured efficiency results of the INV1 and the motor in the failure-condition are slightly improved, and the THD measured results of the output voltage waveforms in the failure-condition of the DC-bus battery are reduced by 67.8% at $m = 0.2$, compared with the normal-condition system.

On the other hand, the proposed fault-tolerant function can generate the 9-level voltage waveforms across the motor windings in $0.25 \leq m < 0.5$ as shown in Fig. 8. Because of the reduction of the harmonic component rate of the output voltage waveforms ,therefore, the measured efficiency results of the INV1 and the motor are also slightly improved, and the THD measured result of the output voltage waveforms in the proposed system is reduced by 52.4% at $m = 0.4$, compared with the normal-condition system.

4.4 SVM Technique to Reduce Error Voltages in Output Voltage Waveforms of Proposed Fault-Tolerant Function The proposed fault-tolerant function, where one of the inverter is operated with the capacitor, has a problem that an unexpected error voltages are generated during a dead time [16][20]. The error voltages are generated due to particular transients of the switching states, where the switching devices in the same phase of both the inverters are synchronously turned on/off, or the several switching devices in one inverter are synchronously turned on/off. Therefore, the synchronous switching technique to reduce the error voltages generated due to the synchronous switching transient is introduced [16][20]. The introduced synchronous switching technique is performed according to the directions of the motor line currents. Therefore, the introduced technique may be incomplete in particular when the line currents are near by the zero-cross points, because it is difficult to detect the directions of the motor line currents. The proposed fault-tolerant function employs the introduced technique.

The conventional switching sequence, for example a triangle wave comparison PWM, has the seven switching states in one PWM sequence. However, the conventional PWM sequence has a problem that the unexpected error voltages are generated during the dead time in the dual inverter drive system, even if the synchronous switching technique is employed. Therefore, the switching sequence to reduce the error voltages is introduced [20]. The introduced sequence has five switching states in one PWM period. In the introduced switching sequence, therefore, the number of switching transitions are less than the conventional sequence, which means that the switching loss is reduced in the introduced sequence. In this paper, the proposed fault-tolerant system is operated with the SVM which employs the introduced sequence. That is why, the introduced sequence also contributes to improve the measured efficiency results of the INV1 and the INV2 in the failure-condition. It is achieved that the measured efficiency results of the motor in the fault-tolerant function is equivalent to the normal-condition. The reason why is that the dv/dt of the output voltage waveforms in the fault-tolerant function is a half of the normal-condition, although the error voltage pulses are generated in the output voltage waveforms of the fault-tolerant function even if the introduced SVM techniques to reduce the error voltages are employed.

5. Conclusion

This paper proposed the fault-tolerant function of the DC-bus battery in the dual inverter drive system. The studied dual inverter drive system has a capacitor in parallel to a battery across the DC-bus of each inverter. In the proposed fault-tolerant function, the failure-side inverter can be achieved the continuous operation with the capacitor instead of the DC-bus battery, even if the DC-bus battery has failed. The proposed fault-tolerant function requires that the capacitor voltage of the failure-side inverter is regulated at a half of the battery voltage of the other inverter and simultaneously the multilevel voltage waveforms are generated to the motor with the SVM. In this paper, the operation characteristics of the proposed fault-tolerant function are examined through the several experimental tests, and the experimental test results are evaluated from the view point of the multilevel voltage waveform generation, the THD measured results of the output voltages to the motor, and the efficiencies of the inverters and the motor, compared with the normal-condition system. Although the transient switching over techniques from the normal-condition to the fault-tolerant functions in the studied dual inverter drive system have not been considered, which will be investigated in detail in future works.

References

(1) A.D. Kiadehi, K.E.K. Drissi, and C. Pasquier: “Voltage THD Reduction for Dual-Inverter Fed Open-End Load With Isolated DC Sources”, IEEE Transactions on Industrial Electronics, Vol.64, No.3, pp.2102–2111 (2017)

(2) B.S. Umeshi and K. Sivakumar: “Dual-Inverter-Fed Pole-Phase Modulated Nine-Phase Induction Motor Drive With Improved Performance”, IEEE Transactions on Industrial Electronics, Vol.63, No.9, pp.5376–5383 (2016)

(3) V.T. Somasekhar, S. Srinivas, and K.K. Kumar: “Effect of Zero-Vector Placement in a Dual -Inverter Fed Open-End Winding Induction-Motor Drive With a Decoupled Space-Vector PWM Strategy”, IEEE Transactions on Industrial Electronics, Vol.55, No.6, pp.2497–2505 (2008)

(4) D. Wu, X. Wu, L. Su, X. Yuan, and J. Xu: “A Dual Three-Level inverter-Based Open-End Winding Induction Motor Drive With Averaged Zero-Sequence Voltage Elimination and Neutral-Point Voltage Balance”, IEEE Transactions on Industrial Electronics, Vol.63, No.8, pp.4783–4795 (2016)

(5) A. Somani, R.K. Gupta, K.K. Mohapatra, and N. Mohan: “On the Causes of Circulating Currents in PWM Drives With Open-End Winding AC Machines”, IEEE Transactions on Industrial Electronics, Vol.60, No.9, pp.3670–3678 (2013)

(6) Y. Kawabata, M. Nasu, T. Nomoto, Emenike C. Ejiogu, and T. Kawabata: “High-Efficiency and Low Acoustic Noise Drive System Using Open-Winding AC Motor and Two Space-Vector-Modulated Inverters”, IEEE Transactions on Industrial Electronics, Vol.49, No.4, pp.783–789 (2002)

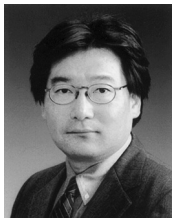
(7) K. Mitsudome, H. Haga, and S. Kondo: “Improvement of Output Voltage Waveform in Dual Inverter Having a Different DC Power Supply”, IEEJ Technical Meeting on Rotating Machinery, Semiconductor Power Converter and Motor Drive, pp.77–82 (2015)

(8) J. Kim, J. Jung, and K. Nam: “Dual-Inverter Control Strategy for High-Speed Operation of EV Induction Motors”, IEEE Transactions on Industrial Electronics, Vol.51, No.2, pp.312–320 (2004)

(9) K.A. Corzine, M.W. Wielevski, F.Z. Peng, and J. Wang: “Control of Cascaded Multi-Level Inverters”, IEEE Transactions on Power Electronics, Vol.19, No.3, pp.732–738 (2004)

(10) H. Machiya, H. Haga, and S. Kondo: "High Efficiency Drive Method of an Open-Winding Induction Machine Driven by Dual Inverter using Capacitor Across DC Bus", IEEJ Transactions on Industry Applications, Vol.135, No.1, pp.10–18 (2015)
(11) J. Ewanchuk, J. Salmon, and C. Chapelsky: "A Method for Supply Voltage Boosting in an Open-Ended Induction Machine Using a Dual Inverter System With a Floating Capacitor Bridge", IEEE Transactions on Power Electronics, Vol.28, No.3, pp.1348–1357 (2013)
(12) S. Chowdhury, P.W. Wheeler, C. Gerada, and C. Patel: "Model Predictive Control for a Dual-Active Bridge Inverter With a Floating Bridge", IEEE Transactions on Industrial Electronics, Vol.63, No.9, pp.5558–5568 (2016)
(13) K.A. Corzine, S. Lu, and T.H. Fikse: "Distributed Control of Hybrid Motor Drives", IEEE Transactions on Power Electronics, Vol.21, No.5, pp.1374–1384 (2006)
(14) Y. Ohto, T. Noguchi, and T. Sasaya: "Space Vector Modulation of Dual Inverter Taking Power Factor of Open-End Winding Motor", IEEJ Annual National Conference, pp.71–72 (2016)
(15) Y. Ohto, T. Noguchi, and T. Sasaya: "Space Vector Modulation of Dual Inverter with Battery and Capacitor across DC Buses", IEEE International Conference on Power Electronics and Drive System, pp.1172–1177 (2017)
(16) A. Mizukoshi and H. Haga: "Control Method of Open-Winding Induction Machine for Improvement of Output Voltage at Low-Modulation Ratio", IEEJ Industry Applications Society Conference, pp.257–260 (2017)
(17) K.K. Nallamekala and K. Sivakumar: "A Fault-Tolerant Dual Three-Level Inverter Configuration for Multipole Induction Motor Drive With Reduced Torque Ripple", IEEE Transactions on Industrial Electronics, Vol.63, No.3, pp.1450–1457 (2016)
(18) W. Zhao, B. Wu, Q. Chen, and J. Zhu: "Fault-Tolerant Direct Thrust Force Control for a Dual Inverter Fed Open-End Winding Linear Vernier Permanent-Magnet Motor Using Improved SVPWM", IEEE Transactions on Industrial Electronics, Vol.65, No.9, pp.7458–7467 (2018)
(19) W. Zhao, Z. Chen, D. Xu, J. Ji, and P. Zhao: "Unity Power Factor Fault-Tolerant Control of Linear Permanent-Magnet Vernier Motor Fed by a Floating Bridge Multilevel Inverter With Switch Fault", IEEE Transactions on Industrial Electronics, Vol.65, No.11, pp.9113–9123 (2018)
(20) Y. Ohto, T. Noguchi, T. Sasaya, T. Yamada, and R. Kazaoka: "Space Vector Modulation of Dual Inverter System Focusing on Improvement of Multilevel Voltage Waveforms", IEEE Transactions on Industrial Electronics, Early Access.

Yoshiaki Oto (Student Member) received the B.Eng. and M.Eng. degrees in Electrical and Electronic Engineering from Shizuoka University, Hamamatsu, Japan in 2015 and 2017, respectively. He has been a Ph.D. student in Department of Environment and Energy Systems, Graduate School of Science and Technology, Shizuoka University since 2017. His research interest is a motor drive technology with a dual inverter system feeding an open-end-winding motor for hybrid vehicles. Mr. Oto is a student member of the Institute of Electrical Engineers of Japan.



Toshihiko Noguchi (Member) received the B.Eng. degree in electrical engineering from Nagoya Institute of Technology, Nagoya, Japan in 1982, and the M.Eng. and D.Eng. degrees in electrical and electronics systems engineering from Nagaoka University of Technology, Nagaoka, Japan, in 1986 and 1996, respectively. In 1982, he joined Toshiba Corporation, Tokyo, Japan. He was a Lecturer at Gifu National College of Technology, Gifu, Japan, from 1991 to 1993. He was an Assistant Professor and an Associate Professor in Department of Electrical, Electronics and Information Engineering, Nagaoka University of Technology from 1994 to 1995 and from 1995 to 2009, respectively. Since 2009, he has been a Professor in Department of Electrical and Electronics Engineering, Faculty of Engineering and Graduate School of Engineering, Shizuoka University. His research interests include new circuit topologies of static power converters and motor drives including electric machine hardware. Dr. Noguchi is a member of the IEE-Japan and a senior member of the IEEE.