

Pure Sinusoidal Output Current-Source Inverter Using New Current Waveform Generation Technique

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Abstract—A novel technique which is able to generate a pure sinusoidal output current waveform for the single-phase current-source inverter is proposed in this paper. The proposed technique incorporates a staircase multilevel current waveform generator and a class-D amplifier-based linear compensating current waveform generator. This linear compensating current is superimposed onto the staircase current waveform in order to reform the output current to a pure sinusoidal waveform. All generated dc link currents are maintained by sensing the load voltage. Therefore, regardless of the load condition, the output current waveform is always constructed on the same number of levels. As a result, the proposed system has efficiency up to 90% and less than 2% output total harmonic distortion without using large output capacitor filter according to computer simulation.

Keywords—current-source inverter; staircase multilevel current; linear compensating current; superimposition; efficiency; harmonics; simulation.

I. INTRODUCTION

Basically, the power inverters are operated based on the switching action in order to optimize the dc-to-ac conversion efficiency, but the output passive filters are indispensable required to reduce the harmonics caused by the switching action. On the other hand, the linear amplifiers can generate a pure sinusoidal waveform, but with very poor power conversion efficiency. Therefore, they are not suitable to be applied as power inverters [1].

The main target for the power converter development is generating pure sinusoidal waveform with low total harmonic distortion (THD) without utilizing large output passive filters and without sacrificing the efficiency. Methods to achieve this goal are either using high-frequency pulse-width modulation (PWM) techniques or employing multilevel techniques. However, each technique has own disadvantage. The high frequency switching techniques lead to high switching losses, while the multilevel techniques lead to high conduction losses [2].

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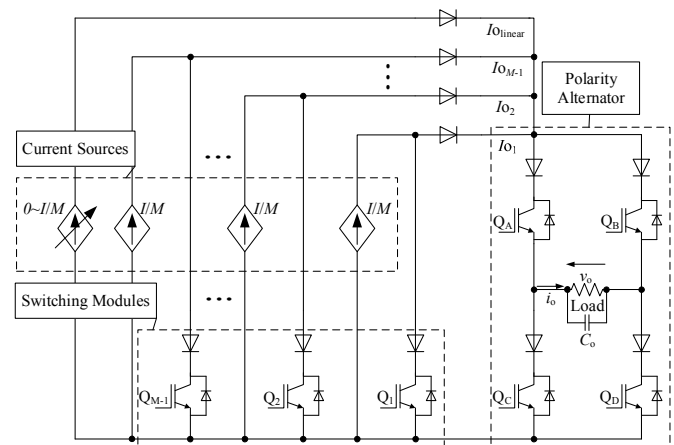


Fig. 1. Generalized concept of hybrid multilevel current-source inverter.

Power inverter can be broadly classified into two types, they are voltage-source inverter (VSI) and current-source inverter (CSI). The VSI system has been widely developed and currently is the most applied in industries. Unfortunately, this kind of inverter will encounter problem while supplying heavy inductive loads such as ac motors. The VSI does not have robust self-protection from short circuit load and has high dv/dt or di/dt transient behavior.

Meanwhile, the current-source inverter (CSI) is less applied due to main disadvantages: high conduction losses and low power density. The highest efficiency can be achieved only if the CSI supplies heavy load. Nonetheless, its advantage such as having natural protection from short circuit and low dv/dt or di/dt cannot be neglected. Therefore, the further CSI development is still required in order to provide an alternative solution in power electronics.

Recently, the authors [3] have reported a new concept of a hybrid multilevel CSI by combining staircase current waveform generator with a linear current waveform generator as described in Fig. 1. However, the actual implementation of the proposed idea is still unclear from the viewpoint of current generation and power source configuration. The system can be improved if only a single power source is used.

This paper proposes new technique to generate pure sinusoidal output for multilevel CSI by adopting Fig. 1 concept. The circuit in Fig. 1 is modified by means of replacing the current source with a buck chopper circuit. Therefore, multiple buck chopper-based current sources can

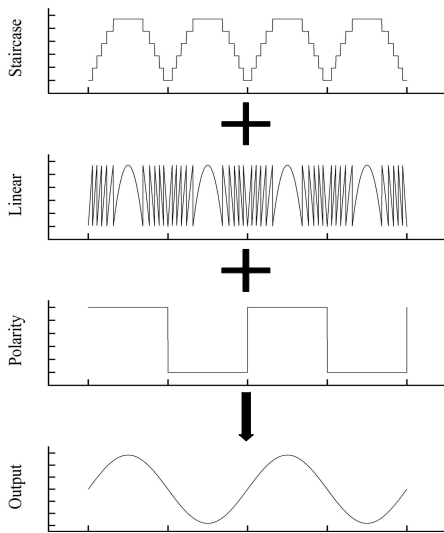


Fig. 2. Operation principle of the hybrid multilevel CSI.

draw power from single power source. The buck choppers which commanded to generate constant current are operated by switching modules to generate staircase current waveform, while the remaining buck chopper is operated using class-D amplifier technique in order to generate linear current.

This paper is organized as follows: first, the operation principle and circuit configuration of the proposed circuit are introduced. Next, the control and switching strategies are elaborated. In order to evaluate and compare the fundamental operation, several multilevel CSI operations of the proposed circuit are demonstrated by computer simulations. From the simulation results, the output current is constructed on the same number of levels regardless of the load condition. Moreover, the THD of the load voltage is still below 2% although a small capacitor is used. And the most important is the efficiency of the proposed system can reach up to 90%.

II. OPERATION PRINCIPLE & CIRCUIT CONFIGURATION

A. Operation Principle

A multilevel CSI is a power electronic device which can provide desired alternating current level at the output using multiple lower level dc currents as an input. Mostly, in the voltage-source inverter topology, a two-level inverter is used in order to generate the ac voltage from dc voltage. On the other hand, in the current-source topology, a high number of levels is needed in order to reduce the conduction losses. As described in Fig. 1, the proposed hybrid multilevel CSI consists of constant current sources, a linear current source, switching modules, and a polarity converter (or inverter) that represented by a H-bridge circuit. The number of the current sources and the switching modules corresponds to the number of CSI levels that expressed by

$$M = (N_{level} - 1) / 2, \quad (1)$$

where the M is defined as the number of stages.

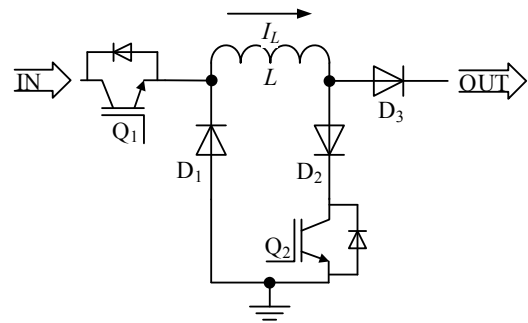


Fig. 3. DC current module circuit.

TABLE I
DC CURRENT MODULE OPERATION PRINCIPLE

Q1	Q2	Output
0	X	0
Switching	0	I_L
X	1	0

X = don't care.

The stage M represents the number of current sources and switching modules that needed by a multilevel CSI system. Each current source generates equal small amount of the constant current, while each switching module preserves the flowing current continuation by whether delivering forward to the load or circulating back to the source.

Fig. 2 illustrates the operation principle of the hybrid multilevel CSI. For this instance, the operation of 13-level is presented. In the case of 13-level, by using (1) the number of required stages is six. The first five stages are used for generating staircase current waveform, meanwhile the remaining one stage is required for generating linear current waveform. In order to generate pure sinusoidal current waveform, after all generated currents are connected in a dc link node, a H-bridge is utilized to alternate the polarity of the current whenever the zero-crossing of the reference is detected. Therefore, all currents are generated in unipolar form and no bipolar source is utilized. Because of using linear current as compensator, a smaller output capacitor is required for smoothing the waveform from high-frequency very-low-amplitude ripples.

B. DC Current Module

As shown in Fig. 1, the dc current sources are indispensable in the CSI system. A dc current source can be constructed by employing dc voltage source buck chopper [4][5][6]. In order to compact the circuit, the switching module part is combined with the buck chopper circuit. This merged circuit is called dc current module as depicted in Fig. 3. The operation principle of this circuit is explained in Table I. As described, this dc current module represents the number of stages M .

The buck chopper part consists of a controlled power switch $Q1$, a smoothing inductor L , and a freewheeling diode $D1$. The chopper switch is used for converting the voltage source to a current source by regulating the dc current flowing through the smoothing inductor. To reduce the smoothing inductor size,

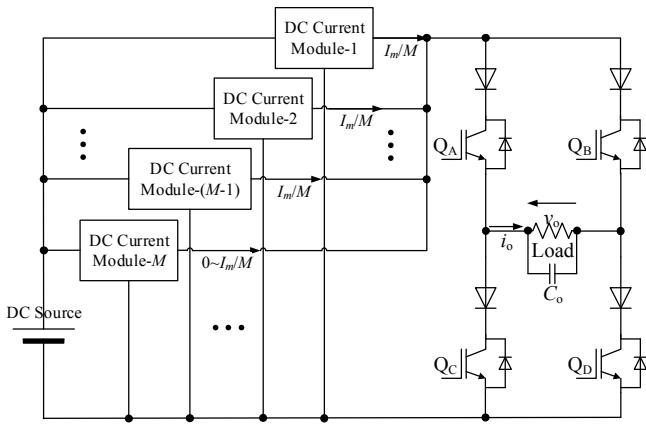


Fig. 4. Proposed design.

the high switching frequency PWM operation is applied. Freewheeling diode is used to keep continuous current flowing through the smoothing inductor.

The switching module part consists of a controlled power switch Q_2 and two reverse-blocking diodes, i.e. D_2 and D_3 . The switching module part directs the current from the smoothing inductor whether flowing forward to the load or circulating back to the chopper. The switching module part works based on the comparison between the absolute value of the reference sinusoidal with the current limit of each stage. Therefore, this part employs low switching frequency operation.

C. Proposed Design

By multiplying the dc current module to the desired number of stages, and then connected with a H-bridge and a power source, the final proposed system is shown in Fig. 4. In this figure, the load is supplied by a current i_o so that gives the load a potential difference of v_o . Because of i_o is ac current, therefore it has a maximum or peak value of I_m where equals to $i_o\sqrt{2}$, and this value is divided equally to several dc current modules that corresponds to the desired level. For example, if the desired level is 13-level, then the I_m is divided by six. The dc current module number 1 through 5 are commanded to generate a constant current of $I_m/6$ amperes, while the dc current module number 6 is commanded to generate linear current that vary from 0 ampere to $I_m/6$ amperes.

D. Conduction Losses of The Proposed System

As explained before that for the N -level CSI with M DC current modules, if the maximum amplitude of N -level output current is I_m , then the flowing current through each DC current module is expressed as

$$I_{DCM} = I_m / M. \quad (2)$$

If each DC current module is assumed to have resistance of R_{DCM} , the module conduction losses (P_{DCM}) caused by this current is expressed as

$$P_{DCM} = I_{DCM}^2 R_{DCM} = \left(\frac{I_m}{M}\right)^2 R_{DCM}. \quad (3)$$

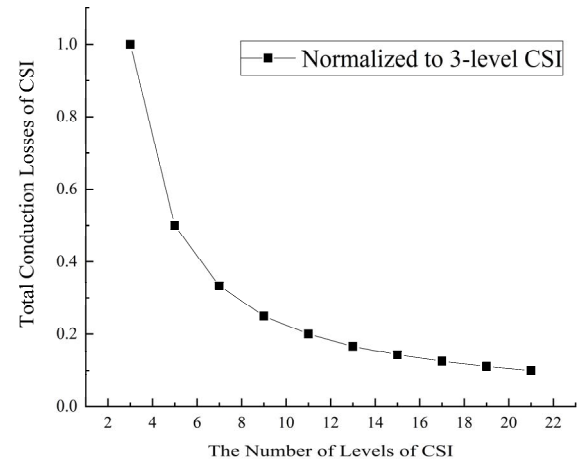


Fig. 5. Conduction losses characteristic of the proposed system.

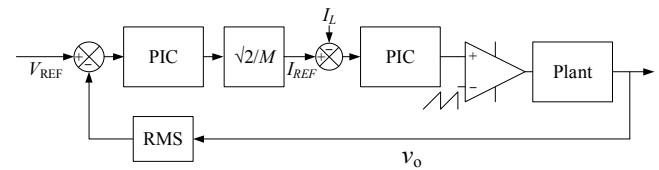


Fig. 6. General scheme of the proposed system current controller.

The total conduction losses due to the DC current modules in a N -level CSI can be expressed as

$$P_{COND_LOSSES} = P_{DCM} \times M = \frac{I_m^2}{M} R_{DCM}. \quad (4)$$

Referring to (1), the lowest N -level number is three. If each conduction losses of several N -level CSI are normalized to 3-level CSI, then the higher number of levels gives lower conduction losses as shown in Fig. 5 [4]. However, the power losses are not only from conduction losses, but also from switching losses. Therefore, it is important to test several multilevel CSIs with different number of levels in order to evaluate and compare the total losses of the proposed circuit.

III. CONTROL & SWITCHING STRATEGIES

A. Output Control

In order to maintain the output stability, the rms value of the load voltage is sensed and controlled. Fig. 6 shows the general scheme of the proposed system controller. This rms value is then subtracted with the voltage reference V_{REF} in order to produce an error. Next, this error is amplified with first proportional-integral (PI) controller to generate rms current reference. In order to determine the peak current value, it has to be multiplied by $\sqrt{2}$. This peak current value is then divided by number of stages M to result the current reference I_{REF} for each buck chopper of the dc current module.

Each buck chopper control scheme is simply subtracting the current reference with the sensed smoothing inductor current and results an error. This error is then amplified with second PI controller to generate PWM reference. Next, this PWM

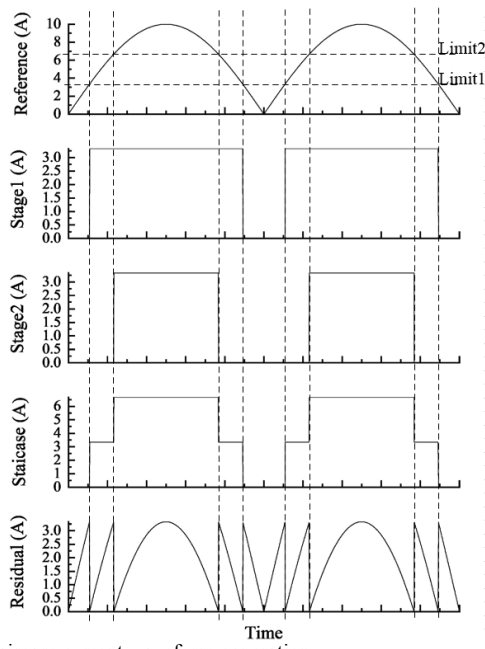


Fig. 7. Staircase current waveform generation.

reference is compared with high-speed frequency sawtooth waveform to generate PWM waveform for corresponding buck chopper.

B. Staircase Current Generator

The staircase current generator works based on the comparison between the reference with the limit of each stage. The reference of this generator is obtained from I_{REF} multiplied by sinusoidal 1 volt ac peak-to-peak. The zero-crossing of this reference signal is used for inverting the polarity of the H-bridge circuit so that the load is supplied by the ac current.

Fig. 7 describes how the staircase current waveform and the linear current reference are generated. After applied as a polarity inverter, the reference is converted to absolute value and becomes a full-wave rectifier waveform. The on-off command for each dc current module depends on the reference that exceed the corresponding limit of each stage. The given limits are from I_{REF}/M to $(M - 1)I_{REF}/M$ consecutively. When the reference exceeds the first limit, it commands the first stage of dc current module to deliver its current to the load as well as subtracts the reference with I_{REF}/M and results a residual reference. Next, when the reference reaches the second stage limit, it triggers the second stage of dc current module as well as subtracts the previous residual reference with I_{REF}/M again and results a new residual reference. This process is carried out repeatedly until the reference exceeds the last limit and the residual reference is completely formed as a linear current reference for class-D amplifier. As shown in Fig. 7, the staircase current waveform is formed from the summation of the outputs of each dc current module.

C. Class-D Amplifier-Based Linear Current Generator

A class-D amplifier or switching amplifier is an electronic amplifier in which the amplifying devices operate as electronic

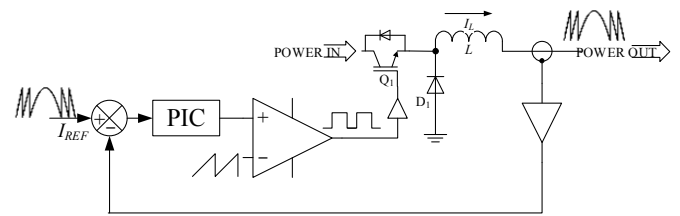


Fig. 8. Class-D amplifier-based linear current generator.

switches, and not as linear gain devices as in other amplifiers [7]. They operate by rapidly switching back and forth between the supply rails, being fed by a modulator using pulse width, pulse density, or related techniques to encode the reference input signal into a pulse train. As depicted in Fig. 8, the most basic way of creating the PWM signal is to use a highspeed comparator that compares a high frequency triangular or sawtooth wave with the reference input. This generates a series of pulses of which the duty cycle is directly proportional with the instantaneous value of the reference signal. The comparator then drives the power switch of the buck chopper part of the last dc current module via a gate driver. This produces an amplified replica of the PWM signal of the comparator. The smoothing inductor removes the high-frequency switching components of the PWM signal and recovers the linear current. In order to make the linear current output accurately and precisely, a current close loop control is applied.

D. Proposed Control System and Overlap Time Compensation

Fig. 9 shows the complete control system for the proposed circuit which is a combination between Fig. 6, the implementation of Fig. 7, and Fig. 8. All terminals of each comparator output are connected to the corresponding power devices of the dc current module that depicted in Fig. 3 and Fig. 4. Technically, this control scheme is divided into five groups of function, they are: (a) output control, (b) buck chopper current control, (c) polarity inverter, (d) staircase current waveform generator, and (e) class-D amplifier-based linear current waveform generator.

In order to preserve the current continuation that always required by CSI system, the polarity inverter includes overlap time compensator which is shown in Fig. 10 [8]. Whenever the polarity changes, it is necessary shorting the H-bridge legs for a few microseconds to avoid the CSI system destruction. The overlap time duration depends on the turn-on and turn-off delays of the utilized switching device.

IV. SIMULATION RESULTS

In order to examine the proper operation of the proposed technique of the multilevel CSI, the 13-level, 17-level, and 21-level CSI configurations, as shown in Figs. 11 – 14, were simulated by PSIM software. The simulation parameters are listed in Table II. There were two types of simulation. First simulation intended to verify the proposed technique could

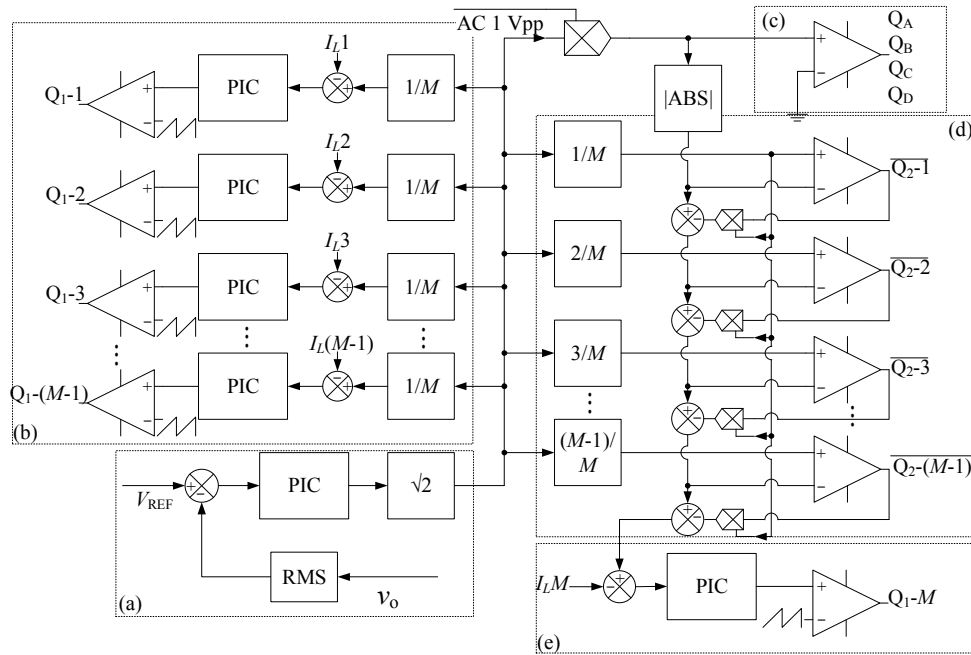


Fig. 9. Proposed control system.

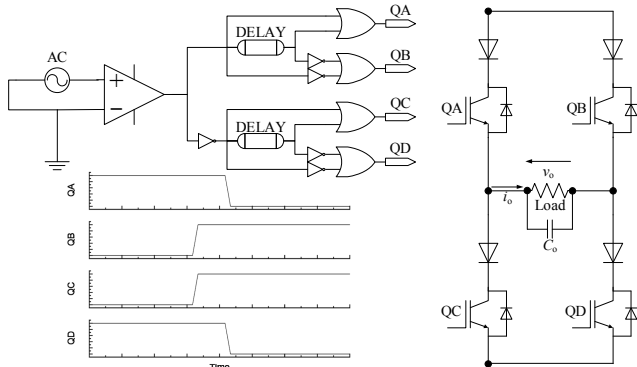


Fig. 10. Overlap time compensation.

give better efficiency and better THD results although using small filter capacitor. To provide the information, the load current and voltage, the load current prior to be filtered, the staircase current and linear current, and the dc input current waveforms are presented.

From the simulation results, it is shown that the load current prior to be filtered by capacitor was a summation between staircase and linear currents. Due to high switching frequency modulation prohibition in the current inversion process, the current was formed in pure sinusoidal with accumulated small ripple at the peak of the waveform. This output waveform is obviously different from the conventional output waveform which was showing high frequency modulation as reported by [4]. Therefore, the utilized output filter capacitor for this proposed system was smaller than utilized in the conventional one.

The second simulation intended to verify the performance of the control system, where the output is maintained precisely and accurately. To perform this simulation, the load was suddenly changed from 10 Ω / 1 mH to 5 Ω / 0.5 mH. Fig. 14

TABLE II
SIMULATION PARAMETERS

DC Voltage	200 V	IGBT V_D	1.0 V
Inductor	560 μH / 0.09 Ω	IGBT R_D	20 mΩ
Filter Capacitor	6.8 μF / 1mΩ	Diode V_F	1.0 V
Load (light)	10 Ω / 1 mH	Diode R_D	20 mΩ
Load (heavy)	5 Ω / 0.5 mH	Sawtooth Freq.	30 kHz
IGBT $V_{CE ON}$	1.4 V	Line Frequency	60 Hz
IGBT $R_{CE ON}$	20 mΩ	Output Voltage	100 V

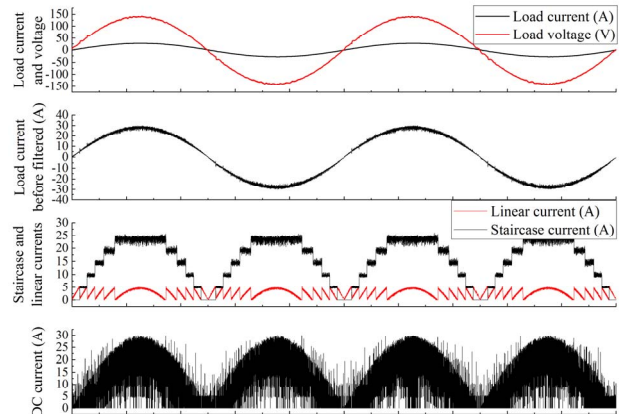


Fig. 11. 13-level CSI simulation result.

shows the dynamic response of the proposed 13-level hybrid multilevel CSI. An excellent transient characteristic of the proposed technique can be confirmed. It is shown that regardless of the load condition, the current was constructed on the same number of levels.

Table III reported the results comparison between 13-level, 17-level, and 21-level CSI from the measured quantities. Despite not significant, the higher number of levels gave better result and the proposed technique has met the requirements.

V. CONCLUSION

A new technique on generating a pure sinusoidal output current for multilevel CSI system using class-D amplifier-based linear compensator has been presented with simulation results. By enlarging the number of levels, the efficiency of the proposed hybrid multilevel CSI can be improved. Because of using the switching-based current source generator, the efficiency can be guaranteed up to 90%.

The linear current compensator gave better THD and led to reduced output filter size. Smaller capacitor is possible to be utilized on the CSI with higher number of levels. In order to verify the simulations, the proposed circuit conducted by proposed technique is currently being investigated in several hardware experimental setups.

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REFERENCES

- [1] T. Noguchi, Y. Iwata and S. Yamaguchi, "Pure sinusoidal output current-source inverter using inductor modules," 2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS), Honolulu, HI, 2017, pp. 869-874.
- [2] B. P. McGrath and D. G. Holmes, "Natural Current Balancing of Multicell Current Source Converters," in IEEE Transactions on Power Electronics, vol. 23, no. 3, pp. 1239-1246, May 2008.
- [3] S. Yamaguchi, T. Noguchi, A. Ikegami, "Hybrid Current-Source Inverter with High-Efficiency Characteristic and Low-Distortion Output," IEEJ Proceedings of Annual Conference, 2013, C4-2.
- [4] Suroso and T. Noguchi, "New H-Bridge Multilevel Current-Source PWM Inverter with Reduced Switching Device Count," Proceeding of IEEJ International Power Electronics Conference, 2010 pp. 1228-1235.
- [5] Suroso and T. Noguchi, "Common-emitter topology of multilevel current-source pulse width modulation inverter with chopper-based dc current sources," in IET Power Electronics, vol. 4, no. 7, pp. 759-766, Aug. 2011.
- [6] T. Noguchi and Suroso, "Review of Novel Multilevel Current-Source Inverters with H-Bridge and Common-Emitter Based Topologies," IEEE Energy Conversion Congress and Exposition, vol. 5, 2010, pp. 4006-4011.
- [7] Y. Kang, T. Ge, H. He and J. S. Chang, "A review of audio Class D amplifiers," 2016 International Symposium on Integrated Circuits (ISIC), Singapore, 2016, pp. 1-4.
- [8] S. Woolaghan and N. Schofield, "Current Source Inverters for PM machine control," 2009 IEEE International Electric Machines and Drives Conference, Miami, FL, 2009, pp. 702-708.
- [9] J. Lai and F. Z. Peng, "Multilevel converter-a new breed of power converters," IEEE Transactions on Industry Applications, vol. 32, no. 5, 1996, pp. 509-517.
- [10] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverter: a survey of topologies, controls, and application," IEEE Trans. on Industrial Electronics, vol. 49, no. 4, p.p. 724-738, August 2002.

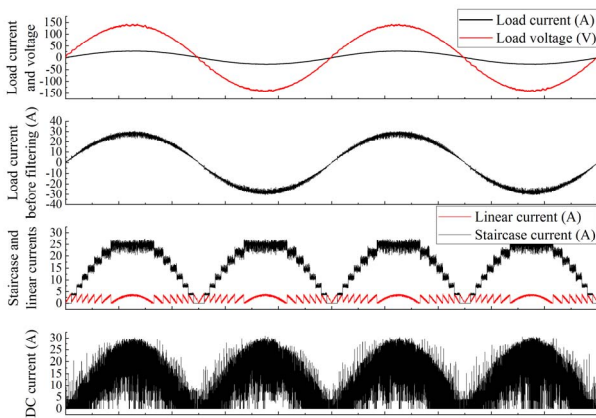


Fig. 12. 17-level CSI simulation result.

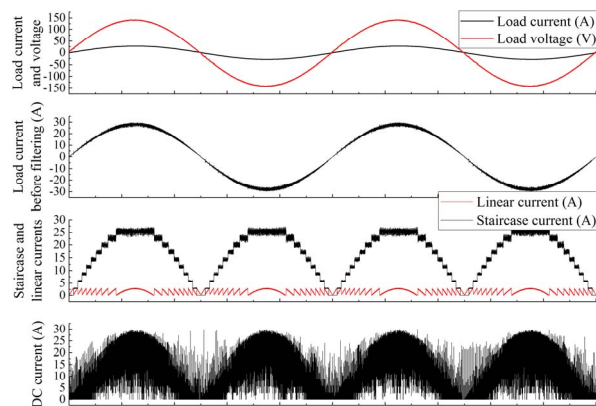


Fig. 13. 21-level CSI simulation result.

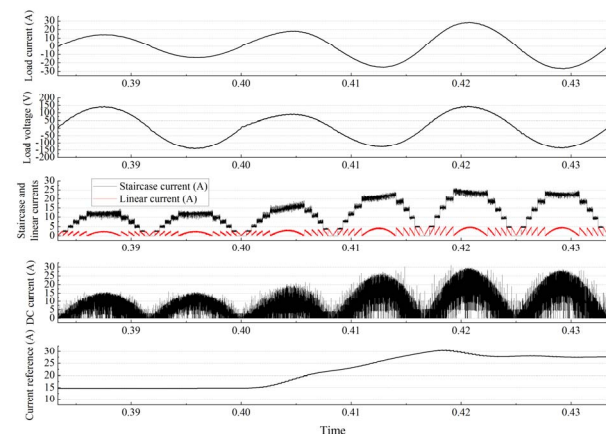


Fig. 14. 13-level CSI dynamic response.

TABLE III
SIMULATION RECORDED DATA

	Number of Levels		
	13-level	17-level	21-level
Load current	20.0 A	20.1 A	20.1 A
Load voltage	100.1 V	100.7 V	100.4 V
DC current	11.2 A	11.3 A	11.2 A
THD-I after filtering	1.65 %	1.03 %	0.56 %
THD-I before filtering	4.19 %	3.45 %	2.87 %
THD-V	1.94 %	1.35 %	0.70 %
Efficiency	89.4 %	89.6 %	90.0 %