Study on Pure Sinusoidal Output Generation Techniques for Single-Phase Current-Source Inverter

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***Abstract*--This paper describes several techniques to create new pure sinusoidal output generation for the current-source inverter (CSI) by incorporating state-of-the-art single-phase multilevel CSIs with linear power amplifiers. The successful key of this hybridization is the superimposition procedure, where the staircase multilevel current is superimposed by the linear compensating current to produce a pure sinusoidal current. The procedure is implemented in DC and AC compensation techniques. By using these strategies, nine new hybrid multilevel CSIs are obtained. One of the new hybrid configurations with DC compensation is tested in the experimental validation to demonstrate the proper operations of the proposed techniques.**

***Index Terms*—hybridization, linear power amplifiers, multilevel current-source inverters, superimposition procedure.**

I. Introduction

Basically, power inverters are operated through a switching action to increase their conversion efficiency. Furthermore, in order to produce very low output harmonic, LC filter usage is indispensable. On the other hand, linear amplifiers can generate a pure sinusoidal waveform with extremely low output harmonic. However, their very low power efficiency makes them inapplicable for the power inverter. The goal for power inverter development is to generate a pure sinusoidal waveform with low output harmonics without using large output passive filter and without sacrificing power efficiency [1].

This study is about once again to promote the current-source inverter (CSI). Their technology development is not so successful as like as voltage-source inverter (VSI) because of two main drawbacks: high conduction losses and low power density caused by inductor-based energy buffer. However, their advantages such as inherent short circuit protection, low dv/dt or di/dt, and simple current control must be considered.

A possible solution to achieve the goal with CSI is by combining a multilevel CSI with a linear amplifier. The multilevel technique enables the power conversion with a very low switching action so that the switching losses in the current inversion process are minimized. The linear amplifier utilization has a function to reform the staircase multilevel current waveform into pure sinusoidal by using the superimposition technique. As a result, a pure sinusoidal current is generated with a very small current ripple. In order to minimize the output current ripple, the proposed system does not have to use a large output filter capacitor. However, this linear amplifier utilization gives a negative impact on the system's total efficiency. In order to reduce the power losses caused by the conduction loss of the linear amplifier circuit, the proposed multilevel CSI must be operated by using a high number of levels [2-5].

II. Proposed Compensation Techniques

In this study, the proposed current superimposition technique is divided into two principles: direct current compensation and alternating current compensation. The direct current compensation is performed by superimposing the staircase multilevel direct current waveform into full-wave direct current prior to the polarity inversion as shown in Figure 1. On the other hand, the alternating current compensation is performed by superimposing the staircase multilevel alternating current waveform into pure sinusoidal. In other words, the superimposition is performed after the current polarity inversion. Figure 2 depicts this proposed AC compensation.

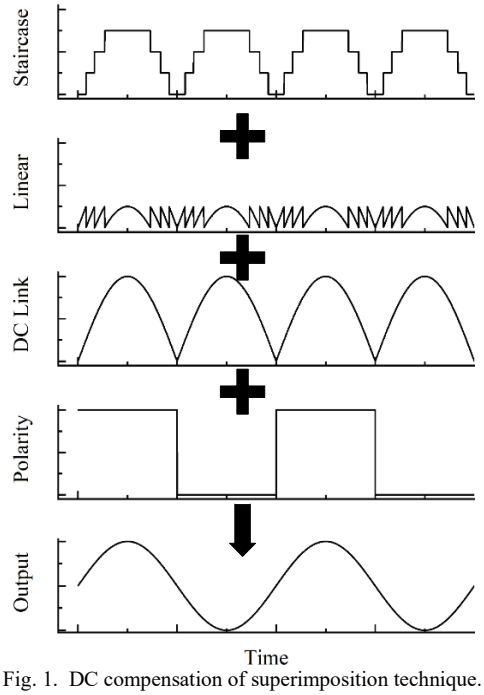

Fig. 1. DC compensation of superimposition technique.

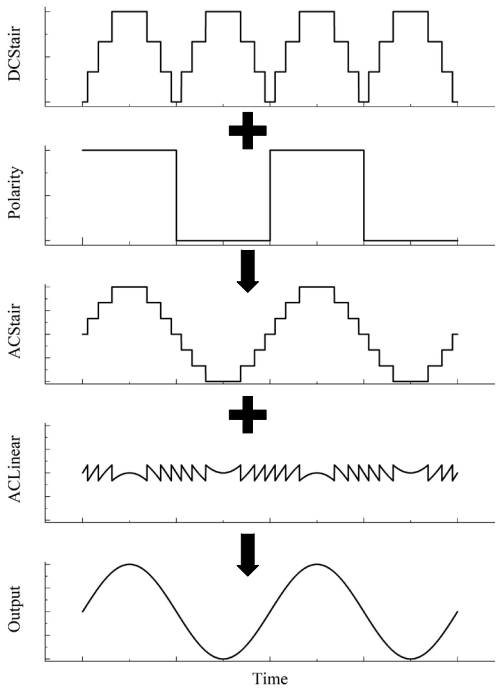

Fig. 2. AC compensation of superimposition technique.

III. Hybridization of the State-of-the-art Single-phase Multilevel CSIs

So far, there have been nine topologies of single-phase multilevel CSI invented. First, common-emitter or fishbone topology multilevel CSI proposed by Suroso and Noguchi [6]. This topology was derived from a neutral point-clamped multilevel voltage-source inverter (VSI) [7] by using the duality principle [8]. The hybridization of this topology is done by installing the two-channel interleaved linear current compensator in the DC side. The 9-level configuration of this hybridization is shown in Figure 3.

The second one is the current-module topology. It was also proposed by Suroso and Noguchi [9] that derived from DC power module topology of multilevel VSI [10] by using the duality principle. The hybridization of this topology is performed by installing the linear current compensator on the DC side. The 9-level configuration of this hybridization is depicted in Figure 4.

The third one is paralleled H-bridge topology. It was derived by using duality from a voltage-source modular multilevel converter. The hybridization of this topology is conducted by installing the linear current compensator on the AC side. The 9-level configuration of this hybridization is illustrated in Figure 5.

The fourth one is single-rating inductor-cell topology, proposed by Xiong [11] and Bai [12]. The hybridization of this topology is done by installing the linear current compensator on the AC side. The 9-level configuration of this hybridization is drawn in Figure 6.

The fifth one is multi-rating inductor-cell with multiple H-bridge or also known as nested inductor-cell, proposed by Bai [12] and McGrath [13] from deriving the flying capacitor multilevel VSI topology. The hybridization of this topology is performed by installing the linear current compensator on the AC side. The 9-level configuration of this hybridization is shown in Figure 7.

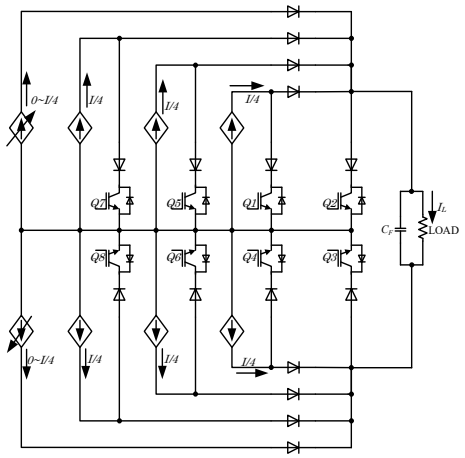

Fig. 3. Hybrid multilevel CSI with common-emitter/fishbone topology.

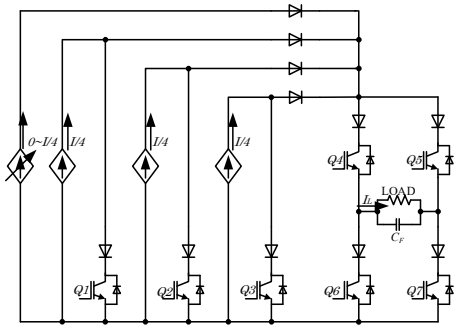

Fig. 4. Hybrid multilevel CSI with current module topology.

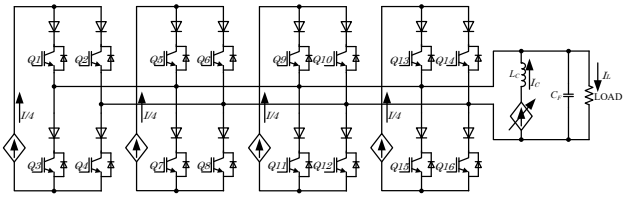

Fig. 5. Hybrid multilevel CSI with paralleled H-bridge topology.

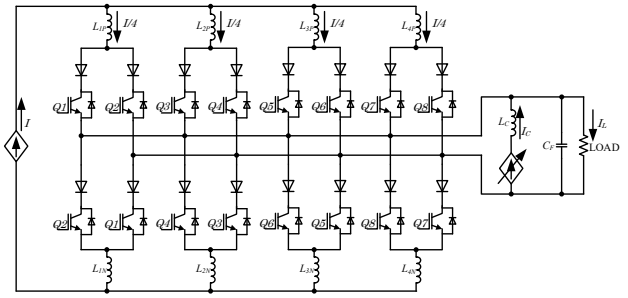

Fig. 6. Hybrid multilevel CSI with single-rating inductor-cell topology.

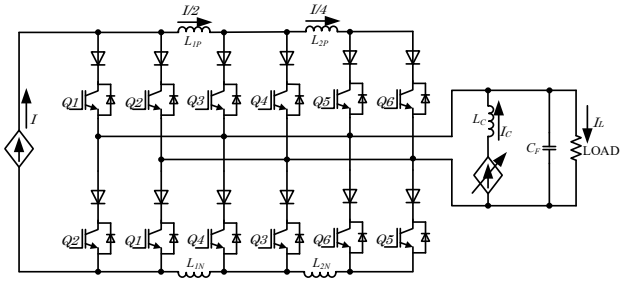

Fig. 7. Hybrid multilevel CSI with nested inductor-cell topology.

The sixth one is multi-rating inductor-cell multiple H-bridge with the reduced device and inductor counts or also known as modified nested inductor-cell, proposed by Vazquez [14] and Bao [15]. The hybridization of this topology is conducted by installing the linear current compensator on the DC side. The 9-level configuration of this hybridization is depicted in Figure 8.

The seventh one is multi-rating inductor-cell with single H-bridge, proposed by Barbosa [16]. The hybridization of this topology is done by installing the linear current compensator on the DC side. The 9-level configuration of this hybridization is depicted in Figure 9.

The eighth one is common-emitter with H-bridge inductor-cell, proposed by Suroso and Noguchi [17]. The hybridization of this topology is performed by installing the linear current compensator on the AC side. The 9-level configuration of this hybridization is depicted in Figure 10.

And the last one is multilevel CSI with H-bridge inductor-cell, proposed by Suroso and Noguchi [18]. The hybridization of this topology is conducted by installing the linear current compensator on the AC side. The 9-level configuration of this hybridization is depicted in Figure 11.

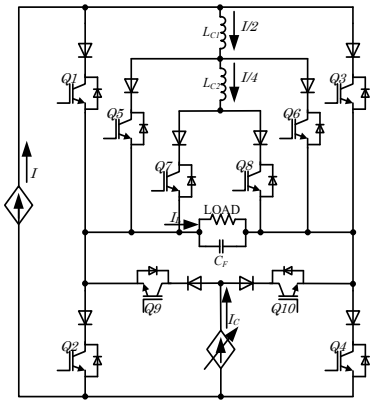

Fig. 8. Hybrid multilevel CSI with modified nested inductor-cell topology.

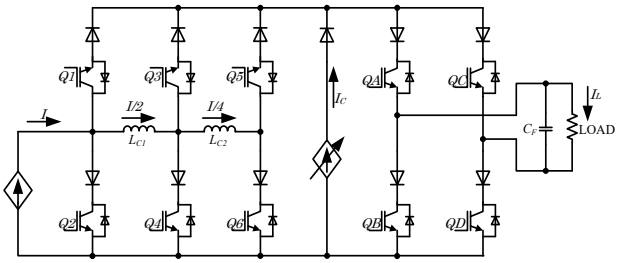

Fig. 9. Hybrid multilevel CSI with single H-bridge multi-rating inductor-cell topology.

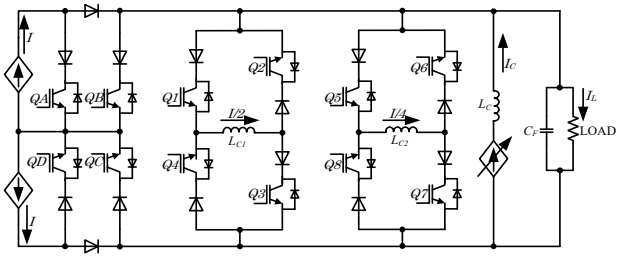

Fig. 10. Hybrid common-emitter multilevel CSI with H-bridge inductor-cell topology.

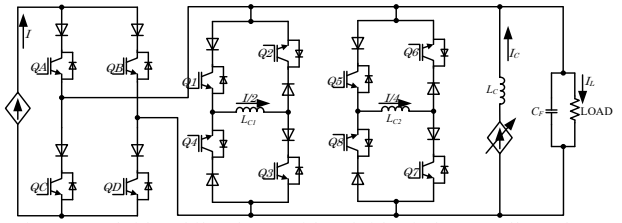

Fig. 11. Hybrid multilevel CSI with H-bridge inductor-cell topology.

TABLE I
DEVICE COUNT COMPARISON BETWEEN PROPOSED HYBRID TOPOLOGIES

Topology	Number of Switches	Number of Diodes	Number of Inductors	Number of Op-Amps	Number of BJTs	Number of Resistors
Figure 3	14	22	6	2	2	2
Figure 4	10	14	3	1	1	1
Figure 5	28	28	4	1	1	1
Figure 6	21	21	9	1	1	1
Figure 7	21	21	7	1	1	1
Figure 8	11	11	3	1	1	1
Figure 9	8	12	3	1	1	1
Figure 10	18	20	4	1	1	1
Figure 11	18	18	3	1	1	1

Table 1 lists the device count comparison of each topology based on the 9-level multilevel CSI circuit. It is shown, Figure 9 topology or multi-rating inductor-cell with single H-bridge has the least number of device count. However, this topology requires an enormous inductor for the main current generator energy buffer that leads to the physical dimension enlargement. In order to make a deeper investigation and experiments with a small prototype and simple implementation, another topology has been chosen; i.e. current module shown in Figure 4. Because the current module topology has the least number of device count without using a large inductor. Due to this topology, the applicable superimposition technique is DC compensation.

IV. IMPLEMENTATION OF THE PRACTICAL DESIGN

Because the actual current source does not exist, it must be constructed from a buck chopper circuit. In order to remove the complexities from creating a cumbersome diagram, the buck chopper circuit and the shorting switch are combined into one circuit called direct current module (DCM) shown in Figure 12.

The current I_L is generated by switching the Q1 at a certain high frequency. In order to direct the current whether supplying the load or circulating back to the source, Q2 is switched in accordance with the comparison of sinusoidal reference and the current limit of each level.

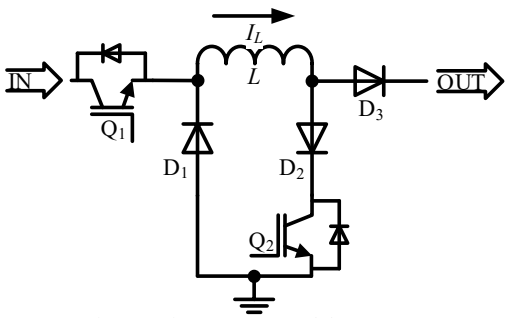

Fig. 12. Direct current module (DCM).

By referring to Figure 4, the number of levels N_{LEVEL} can be determined by

$$N_{LEVEL} = 2M + 1, \quad (1)$$

where M is the number of current sources used in the system or the number of current-fed branches.

Each hybrid multilevel CSI system employs a linear current compensator and several DCMs. And each DCM is subjected to generate a constant current that equals to

$$I_{LIMIT} = \sqrt{2} I_L / M \ \text{(A)}, \quad (2)$$

except for the current compensator which is subjected to generate the current from 0 to I_{LIMIT} Amperes linearly. With this determined current limit, Q1 of each DCM is switched by pulse-width modulation (PWM) signal with a duty cycle equals to $1/M$.

The staircase multilevel current waveform generation follows the mechanism as shown in Figure 13, where the Q2 switching operation is commanded by the result of the comparison of DC full-wave current reference with the I_{LIMIT} on each level. The average value of generated staircase multilevel current can be found by this equation

$$I_{STAIRCASE} = \frac{I_{LIMIT}}{\pi} \sum_{n=1}^{M-1} \left(\pi - 2 \sin^{-1} \frac{n}{M} \right) \text{(A)}, \quad (3)$$

The reference for linear compensating current is produced by simply subtracting the DC full-wave reference with the generated staircase multilevel current waveform as shown in Figure 14. The average value of generated linear compensating current can be found by this equation

$$I_{LINEAR} = \frac{I_{LIMIT}}{\pi} \left[2M - \sum_{n=1}^{M-1} \left(\pi - 2 \sin^{-1} \frac{n}{M} \right) \right] \text{(A)}, \quad (4)$$

Figure 15 shows a linear compensator circuit constructed from a DCM circuit. By disabling Q2 permanently, Q1 is switched by a PWM signal generated from the comparison of linear compensating reference and high-frequency sawtooth carrier waveform.

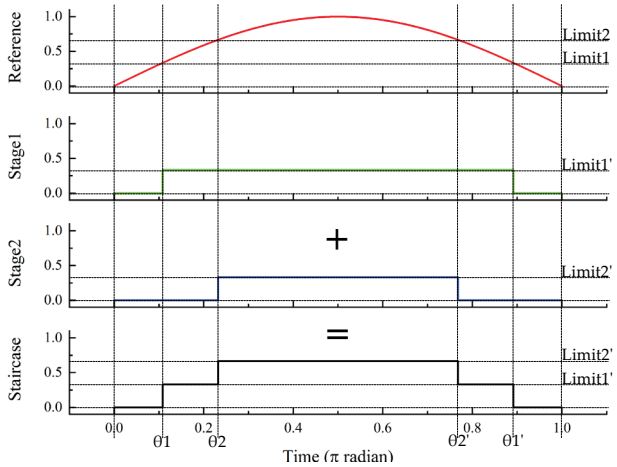

Fig. 13. Staircase multilevel current waveform generation.

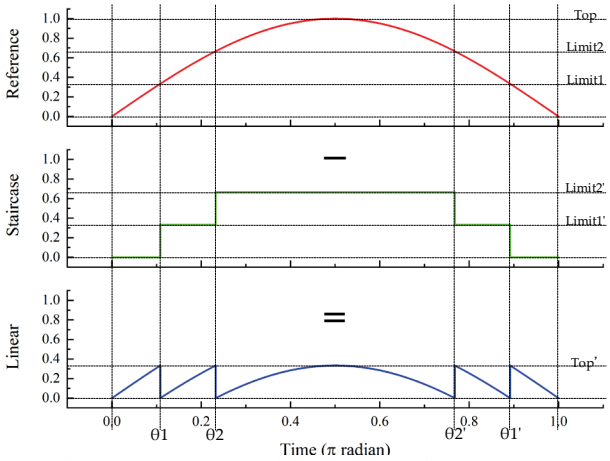

Fig. 14. Linear compensating current waveform generation.

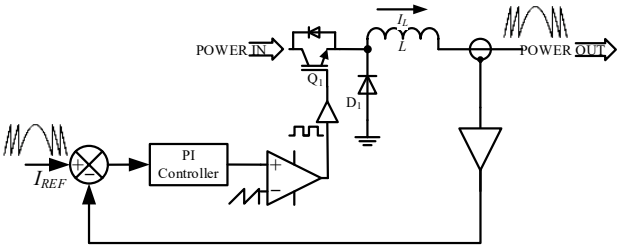

Fig. 15. Linear compensator circuit constructed from DCM.

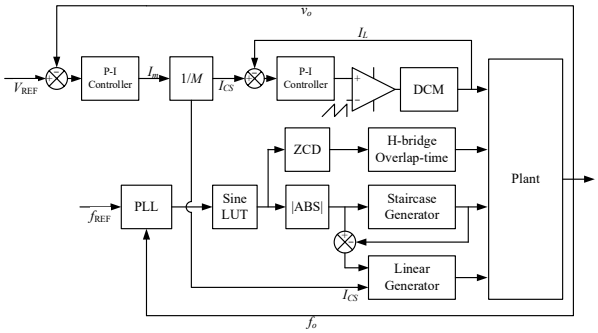

Fig. 16. Control system.

In order to maintain the desired load current, a control system is constructed by combining three closed-loop controllers of output voltage, I_{LIMIT}, and line frequency as shown in Figure 16.

V. Simulation Results & Experimental Validation

In order to verify the proper operation of the proposed hybrid multilevel CSI, PSIM simulations were conducted with determined parameters listed in Table 2.

TABLE II
Simulation Parameters

Parameter	Value
Number of levels (N_{LEVEL})	7, 9, 11, 13, and 15
Number of sources (M)	3, 4, 5, 6, and 7
DC voltage	160 V
Inductor	560 μH/0.09 Ω
Output filter capacitor	6.8 μF/1 mΩ
Load	10 Ω/1 mH, 2 kW max
Sawtooth carrier frequency	50 kHz
Output voltage/frequency	100 V/60 Hz

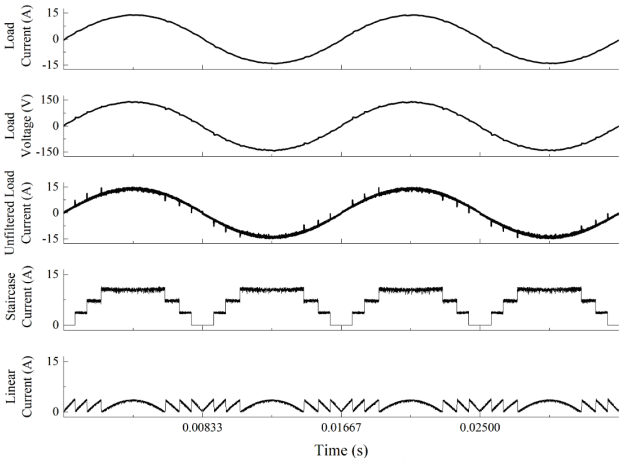

Fig. 17. Operation principle simulation result.

Figure 17 shows the simulation verification of the operation principle of the 9-level proposed hybrid multilevel CSI. The figure consists of the load current, the load voltage, the unfiltered load current, the staircase multilevel current, and the linear compensating current. It is shown that the unfiltered load current is the summation of the staircase and linear currents with the polarity inverter assistance. Due to the multilevel technique application, the current inversion process did not use high-frequency switching modulation. As a result, the unfiltered load current was already a sinusoidal waveform with small ripples. Therefore, the proposed system only needs a small output filter capacitor to eliminate the ripples that lead to a very low output voltage harmonics (THD-V).

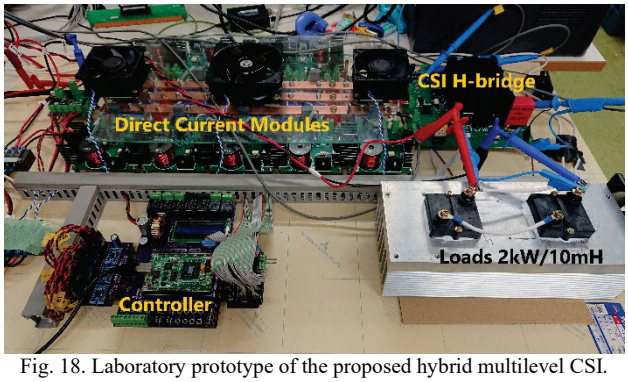

Fig. 18. Laboratory prototype of the proposed hybrid multilevel CSI.

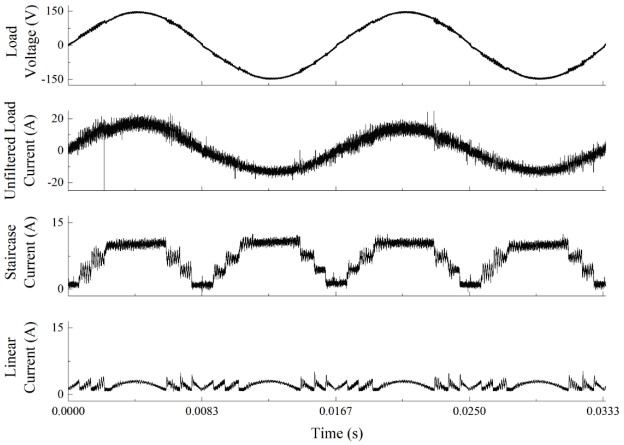

Fig. 19. Operation principle experimental result.

In order to validate the simulation result, experiments with a laboratory prototype shown in Figure 18 were conducted. The prototype consists of an input module, several DCMs, a CSI H-bridge circuit, and an FPGA-based controller. The prototype uses similar parameters as listed in Table 2. The experimental result of the proposed 9-level hybrid multilevel CSI with current module topology is shown in Figure 19. It is shown the proposed technique is successfully applied. In order to compare power efficiency and power quality between simulation and experimental results, Figures 20 and 21 are presented.

Figure 20 shows the comparison of the power efficiency between simulation and experimental results. It is shown that the experimental result is in line with the simulation one. The common finding indicates that efficiency is declining in accordance with the number of levels. Due to switching-based current generator utilization, it is comprehensible that the conduction loss reduction is not significant compared to the other losses such as switching and gate charge losses in a higher number of levels. Moreover, the prototype practical design lack of knowledge makes efficiency never reaches 90%. It should be giving a better result when applied in the better hardware construction and heavier load.

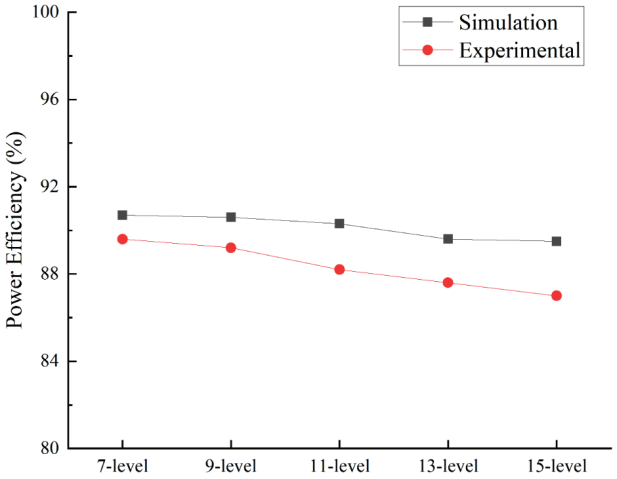

Fig. 20. Power efficiency comparison results.

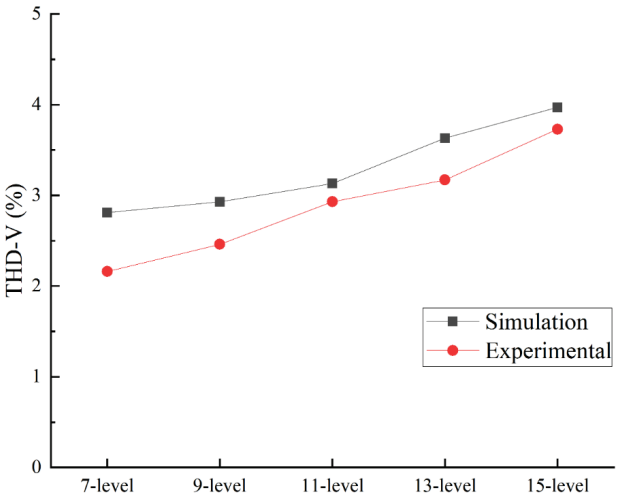

Fig. 21. Power quality comparison results.

On the other hand, Figure 21 shows the comparison of power quality. It is shown that the THD-V experimental result is also in line with the simulation one. It seems the power quality is also declining in accordance with the number of levels. The switching-based current generator utilization causes the current ripples of each level accumulated at the peak of the staircase waveform. This is contrary to the voltage-source type, where on the higher number of levels, the quality becomes better.

VI. Conclusions

A study on pure sinusoidal output generation techniques for single-phase current-source inverter has been discussed by presenting two techniques of superimposition that required for hybridizing the state-of-the-art single-phase multilevel current-source inverters with linear power amplifiers.

One of the techniques has been confirmed by both in the simulation procedure and experimental validation that the proposed technique is successfully applicable with some findings. There was a hypothesis that the higher number of levels application in the multilevel CSI system will reduce the conduction losses. However, the losses are not only conduction but also switching and gate charge losses. It seems that the higher number of levels will generate higher switching and gate charge losses so that the power efficiency results in degrading. In addition, findings also highlight the switching-based current source utilization will degrade the power quality in accordance with the number of levels.

In order to improve power efficiency, the prototype must be re-evaluated. Wide band-gap device application, shortening the copper-based conductors such as bus bars, changing the construction into a round-shape with CSI H-bridge in the middle, and using a very high switching frequency modulation for the buck chopper circuit are further approaches that must be highly considered.

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